

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

LG DISPLAY CO., LTD.,

Plaintiff,

v.

AU OPTRONICS CORPORATION; AU
OPTRONICS CORPORATION AMERICA; CHI
MEI OPTOELECTRONICS CORPORATION,
and CHI MEI OPTOELECTRONICS USA, INC.,

Defendants.

Civil Action No. 06-726 (JJF)

AU OPTRONICS CORPORATION,

Plaintiff,

v.

LG DISPLAY CO., LTD. and
LG DISPLAY AMERICA, INC.,

Defendants.

Civil Action No. 07-357 (JJF)

CONSOLIDATED CASES

LG DISPLAY CO., LTD.,

Plaintiff,

v.

CHI MEI OPTOELECTRONICS
CORPORATION, et al.,

Defendants.

Civil Action No. 06-726 (JJF)

Civil Action No. 07-357 (JJF)

CONSOLIDATED CASES

**DECLARATION OF HUA CHEN
IN SUPPORT OF AUO'S OPENING CLAIM CONSTRUCTION BRIEF**

I, Hua Chen, declare as follows:

1. I am an attorney duly admitted to practice before all the courts of the State of California, and also admitted to practice pro hac vice before this Court. I am an attorney

with the law firm of Paul, Hastings, Janofsky & Walker LLP, counsel of record for Defendants Au Optronics Corporation and Au Optronics Corporation America (collectively "AUO"). I have personal knowledge of the facts declared herein, and if called as a witness, could and would competently testify thereto.

2. I make this Declaration in support of AUO's Opening Claim Construction Brief.

3. Attached hereto as Exhibit "1" is a true and correct copy of selected pages from THE RANDOM HOUSE DICTIONARY OF THE ENGLISH LANGUAGE (2nd Ed. 1987).

4. Attached hereto as Exhibit "2" is a true and correct copy of U.S. Patent No. 4,820,222, issued to S. Holmberg et al. on April 11, 1989.

5. Attached hereto as Exhibit "3" is a true and correct copy of the claim construction opinion issued by Judge J. Farnan on or about June 13, 2006 in *LG. Philips LCD Co., Ltd. v. Tatung Company et al.*, No. 05-292 (JJF) (Del., filed on May 13, 2005) (the "Judge Farnan Memorandum Opinion"). The Judge Farnan Memorandum Opinion addressed certain claim terms and limitation of U.S. Patent No. 5,825,449.

6. Attached hereto as Exhibit "4" is a true and correct copy of selected pages from THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS (4th Ed. 1988).

7. Attached hereto as Exhibit "5" is a true and correct copy of selected pages from RANDOM HOUSE WEBSTER'S COLLEGE DICTIONARY (2nd Ed. 1997).

8. Attached hereto as Exhibit "6" is a true and correct copy of U.S. Patent No. 5,156,986, issued to C. Wei et al. on October 20, 1992 (the "Wei" Reference).

9. Attached hereto as Exhibit "7" is a true and correct copy of U.S. Patent No. 5,036,370, issued to M. Miyago et al. on July 30, 1991 (the "Miyago" Reference).

10. Attached hereto as Exhibit "8" is a true and correct copy of selected pages from the file history of U.S. Patent No. 6,573,127.

11. Attached hereto as Exhibit "9" is a true and correct copy of U.S. Patent No. 7,075,595, issued to H. Moon et al. on July 11, 2006.

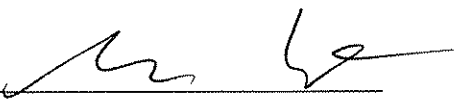
12. Attached hereto as Exhibit "10" is a true and correct copy of selected pages from THE AMERICAN HERITAGE DICTIONARY OF THE ENGLISH LANGUAGE (4th Ed. 2000).

13. Attached hereto as Exhibit "11" is a true and correct copy of selected pages from RANDOM HOUSE WEBSTER'S UNABRIDGED DICTIONARY (2nd Ed. 2001).

14. Attached hereto as Exhibit "12" is a true and correct copy of Japanese patent reference No. 8-171076, along with its English abstract. A copy of the same was included in the file history for U.S. Patent No. 6,803,984.

15. Attached hereto as Exhibit "13" is a true and correct copy of selected pages from THE OXFORD AMERICAN COLLEGE DICTIONARY (2002).

I hereby declare under penalty of perjury under the laws of the United States of America that the matters declared herein are true and correct, and that this declaration is executed this 11th day of August, 2008, at Los Angeles, California.

By 
Hua Chen

CERTIFICATE OF SERVICE

I, Andrew A. Lundgren, Esquire, hereby certify that on August 11, 2008, I caused to be electronically filed a true and correct copy of the foregoing document with the Clerk of the Court using CM/ECF, which will send notification that such filing is available for viewing and downloading to the following counsel of record:

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August 11, 2008

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*Dedicated to the memory of
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Manufactured in the United States of America

rs/uh

depolymerize

de-po-lym-er-ize (dē-pō-līm'ə-rīz', dē-pō-l'ə-mə-), *v.t.*, *-ized*, *-izing*. Chem. to break down (a polymer) into monomers. Also, esp. Brit., *de-po-lym'er-ise*. [1890-95; DE- + POLYMERIZE] —*de-po-lym'er-iza-tion*, *n.*

de-pone (di pōn'), *v.t.*, *-poned*, *-poning*. to testify under oath; depose. [1525-35; < L. *dēponere* to put away, down, aside (ML: to testify), equiv. to *dē-* + *ponere* to put]

de-ponent (di pō'nənt), *adj.* 1. Class. Gk. and Latin Gram. (of a verb) appearing only in the passive or Greek middle-voice forms, but with active meaning. —*n.* 2. Law. a person who testifies under oath, esp. in writing. 3. Class. Gk. and Latin Gram. a deponent verb, as Latin *loqueri*. [1820-30; < L. *dēponēt-* (s. of *dēponēs*) putting away (ML: testifying), prp. of *dēponere*. See *DEPONE*, -*ENT*]

Dep-o-Pro-ve-ra (dēp'ō prō vār'ə), *Pharm.*, Trade-mark. a brand of medroxyprogesterone.

de-pop-u-late (v. dē pōp'yō lāt'; *adj.* dē pōp'yō lit, -lat', *v.* -lat-ed, -lat-ing, *adj.* -lat'. 1. to remove or reduce the population of, as by destruction or expulsion. —*adj.* 2. Archaic. depopulated. [1525-35; < L. *dēpopulātus* devastated (ptp. of *dēpopulāre*), equiv. to *dē-* + *populāre*; see *POPULATE*] —*de-pop-u-la-tion*, *n.* —*de-pop-u-la-tive*, *adj.* —*de-pop-u-la-tor*, *n.*

de-port (di pōrt', -pōrt'), *v.t.* 1. to expel (an alien) from a country; banish. 2. to send or carry off; transport, esp. forcibly. The country deported its criminals. 3. to bear, conduct, or behave (oneself) in a particular manner. [1475-85; < MF *dēporter* < L. *dēportāre* to carry away, banish oneself; equiv. to *dē-* + *portāre* to carry, see *PORT*] —*de-port-a-ble*, *adj.* —*de-port-ee*, *n.* —*de-port-er*, *n.*

de-port-a-tion (dē-pōrt'ā-shən, -pōr-), *n.* 1. the lawful expulsion of an undesired alien or other person from a state. 2. an act or instance of deporting. [1595-96; < L. *dēportatō* (s. of *dēportatō*), equiv. to *dēportat* (us) (ptp. of *dēportāre*; see *DEPORT*, -*ATE*) + *-tō* (-tōn)]

de-port-ment (di pōrt'mənt, -pōrt'), *n.* 1. demeanor; conduct; behavior. 2. the conduct or obedience of a child in school, as graded by a teacher. [1596-1605; < F *déportement*, equiv. to *déporter* (see *DEPORT*) + *-ment* (-ment)] —*Syn.* See *behavior*.

de-pos-al (di pōz'əl), *n.* an act of depositing. [1350-1400; ME; see *DEPOSE*, -*AL*]

de-pose (di pōz'), *v.*, *-posed*, *-pos-ing*. —*v.t.* 1. to remove from office or position, esp. high office. The people deposed the dictator. 2. to testify or affirm under oath, esp. in a written statement; to depose that it was true. —*v.i.* 3. to give sworn testimony, esp. in writing. [1250-1300; ME *deposen* < OF *deposer* to put down, equiv. to *dē-* + *poser* < VL *posere*, LL *posuere*; see *POSSE*] —*de-pos-a-ble*, *adj.* —*de-pos-er*, *n.*

de-posit (di pōz'it), *v.t.* 1. to place for safekeeping or in trust, esp. in a bank account. He deposited his paycheck every Friday. 2. to give as security or in part payment. 3. to deliver and leave (an item). Please deposit your returned books with the librarian. 4. to insert (a coin) in a coin-operated device. Deposit a quarter and push the button. 5. to put, place, or set down, esp. carefully or exactly. She deposited the baby in the crib. 6. to lay or throw down by a natural process; precipitate: The river deposited soil at its mouth. —*v.i.* 7. to be placed, inserted, precipitated, left for safekeeping, given as security or in part payment, etc. —*n.* 8. money placed in a bank account or an instance of placing money in a bank account. 9. anything given as security or in part payment: The boy returned the bottle and got his five-cent deposit back. They made a deposit on the house and signed a ten-year mortgage. 10. anything laid away or entrusted to another for safekeeping: A large deposit of jewels was stolen from the hotel safe. 11. a place for safekeeping; depository. 12. something precipitated, safekeeping, depository. 13. the natural sediment of wine in a bottle. 14. a coating of metal deposited on something, usually by an electric current. 15. a natural accumulation or occurrence, esp. of oil or ore: a mountain range with many rich deposits of gold. [1615-25; < L. *dēpositus* laid down, ptp. of *dēponere*; see *DEPONE*] —*Syn.* 1. bank, save, store. 15. lode, vein, pocket.

de-posit-ary (di pōz'it'ərē), *n.*, *pl.* -tar-ies. 1. one to whom anything is given in trust. 2. depository (def. 1). —*adj.* 3. depository (def. 3). [1595-1605; < LL *dēpositarius* a trustee, equiv. to L. *dēpositus* (see *DEPOSIT*) + *-arius* (-ary)]

de-po-si-tion (dē-pōz'ish'ən, dē-pō-), *n.* 1. removal from an office or position. 2. the act or process of depositing: deposition of the documents with the Library of Congress. 3. the state of being deposited or precipitated: deposition of soil at the mouth of a river. 4. a statement under oath. 5. Law. a. the giving of something under oath. b. the testimony so given. 6. a statement under oath, taken down in writing, to be used in court in place of the spoken testimony of the witness. 7. Eccles. a. the interment of the body of a saint. b. the reinterment of the body or the relics of a saint. 7. (cap.) a work of art depicting Christ being lowered from the Cross. [1350-1400; ME (< AF) < L. *dēpositiō* (s. of *dēpositus*) a putting aside, testimony, burial, equiv. to *dēpositus* (us) laid down (see *DEPOSIT*) + *-tō* (-tōn)] —*de-pō-si-tion-al*, *adj.*

de-pos-it mon-ey. Banking. checks, letters of credit, etc., that circulate and are payable on demand. [1816-25]

de-pos-i-tor (di pōz'it'ər), *n.* 1. a person or thing that deposits. 2. a person who deposits money in a bank or who has a bank account. [1556-65; < LL, equiv. to L. *dēposit-*, var. s. of *dēponere* (see *DEPONE*) + *-tor* (-tor)]

de-pos-i-tory (di pōz'it'ōrē, -tōr'), *n.*, *pl.* -ries. 1. a place where something is deposited or stored, as for safekeeping: the night depository of a bank. 2. a depository; trustee. —*adj.* 3. of or pertaining to a depository; depository: the depository role of a bank. [1650-60;

(def. 1) < ML *dēpositōrium*; (def. 2) *DEPOSIT* + *-ORY* (n. use of *adj.* suffix)]

de-pos-itory li-brary, a library designated by law to receive without charge all or a selection of the official publications of a government. [1925-30]

de-pos-it slip, a slip for listing deposits made to a bank account. Also called *credit slip*. [1900-05]

de-pot (dē-pōt, Mil. or Brit. dep'ōt), *n.* 1. a railroad station. 2. a bus station. 3. Mil. a. a place in which supplies and materials are stored for distribution. b. (formerly) a place where recruits are assembled for classification, initial training, and assignment to active units. 4. a storehouse or warehouse, as a building where freight is deposited. 5. Physiol. a place where body products not actively involved in metabolic processes are accumulated, deposited, or stored. [1785-95; < F *dépôt* < L. *dēpositum*, n. use of neut. of *dēpositus*; see *DEPOSIT*] —*Syn.* 1. 2. terminal.

de-pr. 1. depreciation. 2. depression.

de-prave (di prāv'), *v.t.*, *-praved*, *-praving*. 1. to make morally bad or evil; vitiate; corrupt. 2. Obs. to defame. [1325-75; ME *depraven* (< AF) < L. *dēprāvare* to pervert, corrupt, equiv. to *dē-* + *prāv(us)* crooked + *-are* inf. suffix] —*de-pra-va-tion* (dē-prā vā'shən), *n.* —*de-pra-ver*, *n.* —*de-prav-ing-ly*, *adv.*

de-praved (di prāv'd), *adj.* corrupt, wicked, or perverted. [1585-95; *DEPRAVE* + *-ED*] —*de-praved-ly* (di-prāv'd-lē, -prāv'vīd-), *adv.* —*de-praved-ness*, *n.* —*Syn.* evil, sinful, debased, reprobate, degenerate; dissolute, profligate; licentious, lewd. See *IMMORAL*.

de-prav-ity (di prāv'itē), *n.*, *pl.* -ties. For 2. 1. the state of being depraved. 2. a depraved act or practice. [1635-45; *DEPRAVE* + *-ITY*]

de-pre-cate (dē-prī kāt'), *v.t.*, *-cat-ed*, *-cat-ing*. 1. to express earnest disapproval of. 2. to urge reasons against; protest against (a scheme, purpose, etc.). 3. to pray for deliverance from. [1615-25; < L. *dēprecāre* to pray against, ward off (ptp. of *dēprecari*), equiv. to *dē-* + *precari* (to pray + *-atus* -*ATE*)] —*de-pre-ca-tion*, *n.* —*de-pre-ca-tor*, *n.*

de-pre-ca-tion, *n.* —*de-pre-ca-tor*, *n.* —*Syn.* 1. condemn, denounce, disparage. See *DECRY*. —*Usage.* An early and still the most current sense of *DEPRECATE* is "to express disapproval of." In a sense development still occasionally criticized by a few, *DEPRECATE* has come to be synonymous with the similar but etymologically unrelated word *DEPRECIATE* in the sense "belittle." The author modestly deprecated the importance of his work. In compounds with self-, *DEPRECATE* has almost totally replaced *DEPRECIATE* in modern usage. Her self-deprecating account of her career both amused and charmed the audience.

de-pre-ca-tive (dē-prī kāt'iv, -kāt'iv), *adj.* serving to depreciate; depreciatory. [1480-90; < AF) < LL *dēprecātīvus*, equiv. to *dēprecātus* (see *DEPRECATE*) + *-ivus* (-ive)] —*de-pre-ca-tive-ly*, *adv.*

de-pre-ci-ate (dē-prī kē-tīv, -tōr'), *adj.* 1. of the nature of or expressing disapproval, protest, or depreciation. 2. apologetic; making apology. [1580-90; < L. *dēprecātīvus*, equiv. to L. *dēprecari* (see *DEPRECATE*) + *-tīvus* -*TONY*] —*de-pre-ca-tor-ily*, *adv.* —*de-pre-ca-tor-iness*, *n.*

de-pre-ci-a-ble (di prē'shə bəl, -shə bəl), *adj.* 1. capable of depreciating or being depreciated in value. 2. capable of being depreciated for tax purposes. [*DEPRECATE* + *-ABLE*]

de-pre-ci-ate (di prē'shə āt'), *v.*, *-ated*, *-at-ing*. —*v.t.* 1. to reduce the purchasing value of (money). 2. to lessen the value or price of. 3. to claim depreciation on (a property) for tax purposes. —*v.i.* 4. to represent as of little value or merit; belittle. —*v.t.* 5. to decline in value. [1640-50; < LL *dēprecitātus* undervalued (ptp. of *dēprecare*), in ML *deprecare*, equiv. to L. *dē-* + *precare* (to care for, price + *-atus* -*ATE*)] —*de-pre-ci-at-ing-ly*, *adv.* —*de-pre-ci-a-tor*, *n.*

de-pre-ci-a-tion (di prē'shə ā'shən), *n.* 1. decrease in value due to wear and tear, decay, decline in price, etc. 2. a decrease as allowed in computing the value of property for tax purposes. 3. a decrease in the purchasing or exchange value of money. 4. a lowering in estimation. [1730-40, Amer.; *DEPRECATE* + *-ION*]

de-pre-ci-a-tory (di prē'shə ā-tōrē, -tōr'), *adj.* tending to depreciate. Also, *de-pre-ci-a-tive* (di prē'shə ā-tīv, -shə tīv). [1795-1805; *DEPRECATE* + *-ORY*] —*de-pre-ci-a-tive-ly*, *adv.*

de-pre-date (dē-prī dāt'), *v.*, *-dat-ed*, *-dat-ing*. —*v.t.* 1. to plunder or lay waste to; prey upon; pillage; ravage. —*v.i.* 2. to plunder; pillage. [1620-30; < LL *dēpradātus* plundered (ptp. of *dēpradare*), equiv. to L. *dē-* + *pradare* (to plunder (see *PREY*) + *-atus* -*ATE*)] —*de-pra-dat-or*, *n.* —*de-pra-da-tory* (dē-prī dāt'ōrē, -tōr'), *adj.*

de-pre-da-tion (dē-prī dā'shən), *n.* the act of preying upon or plundering; robbery; ravage. [1475-85; < LL *dēpradātō* (s. of *dēpradātus*) a plundering, equiv. to *dēpradātus* (see *DEPRADATE*) + *-tō* (-tōn)] —*de-pra-da-tion-ist*, *n.*

de-press (di pres'), *v.t.* 1. to make sad or gloomy; lower in spirits; deject; despirit. 2. to lower in force, vigor, activity, etc.; weaken; make dull. 3. to lower in amount or value. 4. to put into a lower position: to depress the muzzle of a gun. 5. to press down. 6. Music. to lower in pitch. [1275-1325; ME *depressen* < AF, OF *depresser* < L. *dēpressus* pressed down (ptp. of *dēprimere*, equiv. to *dē-* + *primere*, comb. form of *primere* to press), see *PRESSURE*] —*de-press-ible*, *adj.* —*de-press-ib-ly*, *adv.*

de-press-ant (di pres'ənt), *adj.* 1. Med. having the quality of depressing or lowering the vital activities; sedative. 2. causing a lowering in spirits; dejecting. —*n.* causing a drop in value; economically depressing.

4. Med. a sedative. Cf. *stimulant* (def. 1). 5. Ch. agent capable of diminishing a specific property or stance. [1675-80; *DEPRESS* + *-ANT*]

de-pressed (di pres't'), *adj.* 1. sad and gloomy; dejected; downcast. 2. pressed down, or situated below the general surface. 3. lowered in force, etc. 4. undergoing emotional hardship, esp. poverty, unemployment. 5. being or measured below the normal or norm. 6. Bot., Zool. flattened down; gr. width than in height. 7. Psychiatry. suffering from depression. [1375-1425; late ME; see *DEPRESS*, -*ED*] —*Syn.* 1. saddened, morose, despondent, miserable; morbid. —*Ant.* 1. happy.

de-pressed' ar'ea, a region where unemployment and a low standard of living prevail. [1925-30]

de-press-ing (di pres'ing), *adj.* serving to depress; causing a state of depression; depressing news. [*DEPRESS* + *-ING*] —*de-press-ing-ly*, *adv.*

de-press-ion (di presh'ən), *n.* 1. the act of depressing. 2. the state of being depressed. 3. a depressed area or place; a place lower than the surrounding surface. 4. sadness; gloom; dejection. 5. a condition of general emotional dejection and drawn sadness greater and more prolonged than warranted by any objective reason. Cf. *clinical depression*. 6. dullness or inactivity, as of trade. 7. period during which business, employment, and market values decline severely or remain at a low level of activity. 8. the Depression. See *GREAT DEPRESSION*. 9. Pathol. a low state of vital powers or function. 10. Astron. the angular distance of a body below the horizon; negative altitude. 11. the angle between the line from an observer or ment to an object below either of them and a horizontal line. 12. Phys. Geog. an area completely or more rounded by higher land, ordinarily having a drainage not conforming to the valley of a stream. 13. Meteorol. an area of low atmospheric pressure. [1350-1400; ME (< AF) < ML *dēpressiō* (depression), LL: a pressing down, equiv. to L. *dē-* + *pressere* (see *DEPRESS*) + *-iō* (-tōn)] —*Syn.* 4. discouragement, despondency.

Depres'sion glass, inexpensive, machine-made usually translucent glassware, including drinking vessels, etc., mass-produced in the U.S. from the 1920's to the 1940's and often used as giveaways; induce customers to buy goods or movie tickets.

de-pres-sive (di pres'iv), *adj.* 1. tending to depress. 2. characterized by depression, esp. mental depression. 3. a person suffering from a depressive disorder. [1810-20; *DEPRESS* + *-IVE*] —*de-pres-sive-ly*, *adv.* —*de-pres-sive-ness*, *n.*

de-press-o-mo-tor (di presh'ō mō'tōr), *adj.* F. Med. causing a retardation of motor activity; de motor nerves. [*DEPRESS* + *-O-* + *motor*]

de-press-or (di pres'ər), *n.* 1. a person or thing that depresses. 2. Surg. an instrument for pressing or protruding part, as a tongue depressor. 3. A muscle that draws down a part of the body, as the muscle of the mouth. Cf. *levator*. 4. Also called *depressor nerve*, a nerve that, when stimulated, induces increase in activity, as a slowed heartbeat. [1605 LL, deriv. of L. *dēprimere* (see *DEPRESS*, -*TOR*)]

de-pressur-ize (dē presh'ə-rīz'), *v.*, *-ized*. —*v.t.* 1. to remove the air pressure from (a pressurized compartment of an aircraft or spacecraft). 2. to relieve the tensions of, cause to relax: A week's vacation depressurized me. —*v.i.* 3. to lose air pressure: The plane cabin depressurized almost instantly. *Altitude depressurizer*. [1940-45; *DE-* + *pressurize*]

de-priv-a-tion (dē-prī vā'shən), *n.* 1. the act of depriving. 2. the fact of being deprived. 3. dispossession. 4. removal from ecclesiastical office. 5. pri- loss. [1525-35; < ML *dēprivatō* (s. of *dēprivatō*), equiv. to *dē-* + *privare* (to deprive (ptp. of *dēprivare*; see *DEPRIVE*) + *-tō* (-tōn)]

de-priv-e (di prīv'), *v.t.*, *-priv-ed*, *-priv-ing*. 1. to move or withhold something from the enjoyment of (a person or persons); to deprive a man of his office. [1275-1325; ME *depriven* < AF, OF *dē-* + *privare*, equiv. to L. *dē-* + *privare* (to deprive (ptp. of *dēprivare*; see *DEPRIVE*) + *-are* inf. suffix)] —*de-priv-able*, *adj.* —*de-priv-al*, *n.* —*de-priv-a-tive* (di-prīv'at-iv), *adj.* —*de-priv'er*, *n.*

de-priv-ed (di prīv'd), *adj.* marked by deprivation; lacking the necessities of life, as adequate food and shelter: a deprived childhood. [1645-55; *DEPRIVE* + *-ED*]

de-pro-fes-sion-al-ize (dē-prō fesh'ə-nīz'), *v.*, *-ized*, *-izing*. 1. to remove from professional or influence, manipulation, etc. 2. to cause to become unprofessional; discredit or deprive of professional status: a campaign to deprofessionalize the doctors. Also, esp. Brit., *de-pro-fes-sion-nal-ize*. [1880-85; *DE-* + *PROFESSIONALIZE*]

de-pro-fund-is (dē prō fōn'dīz), Latin. out depths (of sorrow, despair, etc.).

de-pro-gram (dē prō'gram), *v.t.*, *-gram-med*, *-gram-ming* or *-gram-ing*. 1. to free (a system) from the influence of a religious cult, political doctrine, etc., by intensive persuasion or reeducation. 2. to retrain, as for the purpose of eliminating or having a learned or acquired behavior pattern or habit that is undesirable or unsuitable. [1970-75, Amer.; *PROGRAM*] —*de-pro-gram-mer*, *de-pro-gram-er*, *n.*

de-psi-de (dēpsīd, -sid), *n.* Chem. any of a group of organic compounds.

CONFER MORNINGUATION KEY: act, cape, dare, part; set, equ. ex, over, order, oil, both, out; out, argu, child; sing; sh. that, as in treasure, a = as in alone, e as in system, easily, o as in gallop, u as in circus; * as in (fr) (fr), how and n can serve as syllabic components, as in cradle (krād but'n). See the full key inside the front cover.

Prospect Heights

1553

experimentally in order to test its value. —v.t. 1.4. to search or explore a region for gold or the like. [1400-50; ME *prospere* < L. *prospere* outlook, view. See *prospere*.]
prospectless, adj. —*prospec-tor* (pro-spek'tor, pro-spek'tor), n.
 —Syn. 6, 7. See view, 7, 8, perspective.

Prospect Heights, a town in N Illinois. 11,808.
prospective (pro-spek'tiv), adj. 1. of or in the future: prospective earnings. 2. potential, likely, or expected: a prospective partner. [1880-90; < L. *prospectivus*. See *prospere*, -ive]. —*prospec-tive-ly*, adv.
 —*prospec-tive-ness*, n.

prospectus (pro-spek'tus), n., pl. -tus-es. 1. a document describing the major features of a proposed literary work, project, business venture, etc., in enough detail that prospective investors, participants, or buyers may evaluate it: Don't buy the new stock offering until you read the prospectus carefully. 2. a brochure or other document describing the major features, attractions, or services of a place, institution, or business to prospective patrons, clients, owners, or members. [1770-80; < L. *prospere* outlook, view, equiv. to *prospere*, s. of *prospere* (pro-spek'tor) + *specere*, comb. form of *specere* to look + *pro-* suffix of v. action]

prosper (pro-sper), v.t. 1. to be successful or fortunate, esp. in financial respects; thrive; flourish. —v.t. 2. Arelatic to make successful or fortunate. [1425-75; late ME *prosperen* < L. *prosperare* to make happy, deriv. of *prosperus* PROSPEROUS]. —Syn. 1. See succeed. —Ant. 1. fail.

prosperity (pro-sper-i-ti), n., pl. -ties. 1. a successful, flourishing, or thriving condition, esp. in financial respects; good fortune. 2. *prosperitas*, prosperous circumstances. [1175-1225; ME *prosperite* < OF < L. *prosperitas*. See *prosperus*, -ity].

prospero (pro-spe-ro), n. (in Shakespeare's *The Tempest*) the exiled Duke of Milan, who is a magician.

prosperous (pro-sper-es), adj. 1. having or characterized by financial success or good fortune; flourishing; successful: a prosperous business. 2. well-to-do or well-off: a prosperous family. 3. favorable or propitious. [1400-50; late ME < L. *prosperus*] —*pros-perous-ly*, adv. —*pros-perous-ness*, n.
 —Syn. 1. thriving. 2. wealthy, rich. 3. fortunate, lucky, auspicious.

prosphora (Gk. *prosphōra*; Eng. *pros-fō-rā*, -fer-ə), n. Eastern Ch. antidoron. [1870-75; < Gk. *prosphōra* an offering, lit., a bringing to, applying, equiv. to *pro-* toward + *phōra* something carried (verb. of *pherein* to bring)]

prosphoron (Gk. *prosphōron*; Eng. *pros-fō-ron*, -fer-en), n. Eastern Ch. an uncut loaf of altar bread before it is consecrated. [< Gk. *prosphōron*, n. use of neut. of *prosphoros* useful, fitting, deriv. of *prosphōra* PROSPHORA]

pross (pros), v.t. Scot and North Eng. to exhibit pride or haughtiness; put on airs. [perh. Scots var. in v. use, of *prossess*] —*pross-er*, n. —*pross-ly*, adj.

pross (pros), n. Slang. prostitute. [by shortening and resp.]

Prosser (pros-er), n. Gabriel, 1775-1800, U.S. leader of unsuccessful slave revolt.

prost (prōst), interj. prosit. [by contr.]

prosta-cy-clin (pro-sta-sik-lin), n. Biochem. a proaglandin, C₁₉H₃₂O₆, that specifically inhibits the formation of blood clots. [1975-80; *prostata* (n.) + *cyclin* (n.) on the model of PROTAGLANDIN]

prosta-glan-din (pro-sta-glan-din), n. 1. Biochem. any of a class of unsaturated fatty acids that are involved in the contraction of smooth muscle, the control of inflammation and body temperature, and many other physiological functions. 2. Pharm. any commercial preparation of this substance. [1935-40; *prostata* (n.) + *oland* + -in]

pro-stas (prō-stas), n., pl. *pro-sta-des* (prō-stā-dēz). 1. (in classical architecture) an antechamber or vestibule. 2. (in a classical temple) the area included between parastades. [< Gk. *prostas* lit., that which stands before (cf. *prostasis*)]

pro-sta-sis (prō-stā-sis), n., pl. -ses (-sēz). (in a classical temple) a pronao or prosta before a cella. [< Gk. *prostasis*; see *pro-*, -stasis]

pro-sta-te (pros-tāt), Anat. —adj. 1. Also, *pro-static* (pro-stat-ik), of or pertaining to the prostate gland. —n. 2. See prostate gland. [1840-50; < NL *prostatā* < Gk. *prostatis* one standing before. See *pro-*, -statis]

pro-sta-tec-to-my (pros-tā-tek'tō-mē), n., pl. -mies. Surg. excision of part or all of the prostate gland. [1880-90; *prostatē* + -ectomy]

pro-sta-te gland, Anat. an organ that surrounds the urethra of males at the base of the bladder, comprising a muscular portion, which controls the release of urine, and a glandular portion, which secretes an alkaline fluid that makes up part of the semen and enhances the motility and fertility of sperm. [1830-40]

prostat-ic u-tricle, Anat. a small pouch near the prostate gland that opens into the urethra. [1920-25]

prosta-tism (pro-stat-iz-əm), n. symptoms of prostate disorder, esp. obstructed urination, arising from benign enlargement or chronic disease of the prostate gland. [1895-1900; *prostatē* + -ism]

prosta-titis (pro-stat-itis), n. Poitol. inflammation of the prostate gland. [PROSTATIS + -itis]

pro-ster-num (prō-stēr-nem), n., pl. -na (-nə), -num. The ventral surface of the prothorax of an insect. [1820-30; < NL; see *pro-*, -sternum] —*pro-ster-nal*, adj.

pro-Nor-dic, adj.
pro-North, n., adj.
pro-North-ern, adj.
pro-Nor-west, n., adj.
pro-op-er-a, adj.

pro-O-ri-on-tal, adj., n.
pro-or-tho-dox, adj.
pro-or-tho-dox-y, adj.
pro-pae-tism, n.
pro-pae-tist, n., adj.

pro-the-sis (pro-thē-sis for 1; pro-thē-sis for 2), n., pl. -ses (-sēz for 1; -sēz for 2). 1. a device, either external or implanted, that substitutes for or supplements a missing or defective part of the body. 2. Gram., Prosody, the addition of one or more sounds or syllables to a word or line of verse, esp. at the beginning. [1545-50; < L. < Gk. *prothesis* a putting to, addition, equiv. to *pro-* to + *thesis* a placing; see *thesis*] —*pro-thet-ic* (pro-thet-ik), adj. —*pro-thet-i-cal-ly*, adv.

prosth-et-ic den-tistry, prosthodontics.

prosth-et-ic group, Biochem. the nonprotein acid constituent of a conjugate protein, as the heme group of hemoglobin. [1895-1900]

prosth-et-ics (pro-thet-iks), n. (used with a singular or plural v.) 1. the branch of surgery or of dentistry that deals with the replacement of missing parts with artificial structures. Cf. *prosthodontics*. 2. the fabrication and fitting of prosthetic devices, esp. artificial limbs. [1890-95; see *prosthesis*, -ics]

prosth-et-ist (pro-thet-ist), n. a person skilled in making or fitting prosthetic devices. [1900-05; *prosthesis* (n.) + -ist]

prosth-ion (pro-thē-on), n. Craniom. the most forward projecting point of the anterior surface of the upper jaw, in the midsagittal plane. [1920-25; < Gk. *prosthion*, neut. of *prosthios* frontal, akin to *prosthēn* forward] —*prosth-ion-ic*, adj.

prosthodon-tics (pro-thē-don'tiks), n. (used with a singular v.) the branch of dentistry that deals with the restoration and maintenance of oral function by the replacement of missing teeth and other oral structures by artificial devices. Also, *prosthodontia* (pro-thē-don'shē, -shēz). [1945-50; *prosthesis* + -odont + -ics]

prosthodon-tist (pro-thē-don'tist), n. a specialist in prosthodontics. [1915-20; *prosthodontics* (n.) + -ist]

prostitute (pro-sti-tūt), n. Slang. a prostitute. [PROSTITUTE + -it]

Prostig-min (prō-stig'min), Pharm. Trademark. a brand of neostigmine.

pro-sti-tute (prō-sti-tūt), n., v., -tut-ed, -tut-ing. —n. 1. a woman who engages in sexual intercourse for money; whore; harlot. 2. a man who engages in sexual acts for money. 3. a person who willingly uses his or her talent or ability in a base and unworthy way, usually for money. —v.t. 4. to sell or offer (oneself) as a prostitute. 5. to put to any base or unworthy use: to prostitute one's talents. [1520-30; < L. *prostituta*, n. use of fem. of *prostitutus*, ptp. of *prostitui* to expose (for sale), equiv. to *pro-* + *stitui*, comb. form of var. s. of *statuere* to cause to stand + -tus ptp. suffix; see *status*] —*pro-sti-tu-tor*, n.
 —Syn. 1. call girl, streetwalker, courtesan, trollop, strumpet.

prosti-tu-tion (prō-sti-tū'shən, -tūt-ē-shən), n. 1. the act or practice of engaging in sexual intercourse for money. 2. base or unworthy use, as of talent or ability. [1545-55; < L. *prostitutio* (s. of *prostitui*). See *prostitute*, -tion]

pro-sto-mi-nal (prō-stō-mē-nəl), adj. having a pro-stomium. [1885-90; *prostromi* (um) + -ate]

pro-sto-mi-num (prō-stō-mē-nəm), n., pl. -mi-na (-mē-nə). the unsegmented, preoral portion of the head of certain lower invertebrates. [1866-70; < NL < Gk. *prostomion* mouth. See *pro-*, -stoma, -ium] —*pro-sto-mi-nal*, adj.

pro-sto-on (prō-stō-on), n., pl. -sto-na (-stō-nə). (in classical architecture) a portico. [< Gk. *prostōon*; see *pro-*, -stoa]

pro-strate (pros-trāt), v., -trated, -trating. adj. —v.t. 1. to cast (oneself) face down on the ground in humility, submission, or adoration. 2. to lay flat, as on the ground. 3. to throw down level with the ground. 4. to overthrow, overcome, or reduce to helplessness. 5. to reduce to physical weakness or exhaustion. —adj. 6. lying flat or at full length, as on the ground. 7. lying face down on the ground, as in token of humility, submission, or adoration. 8. overthrown, overcome, or mission. 9. a country left prostrate by natural disasters. 10. helplessly weak or exhausted. 11. submissive. 12. Bot. (of a plant or stem) lying flat on the ground. [1801-1400; (adj.) ME *prostrat* < L. *prostratus*, ptp. of *prostrare* to throw prone, equiv. to *pro-* + *strā-*, var. s. of *sternere* to stretch out + -tus ptp. suffix; (v.) ME *prostraten*, deriv. of the adj.] —*pro-strat-ive* (pros-trā-tiv), adj. —*pro-strator*, n.

prostrat-ion (pros-trā-ti-shən), n. 1. the act of prostrating. 2. the state of being prostrated. 3. extreme mental or emotional depression or dejection; nervous prostration. 4. extreme physical weakness or exhaustion; heat prostration. [1820-30; < L. *prostratio* (s. of *prostrare*) a lying prone. See *prostrare*, -ion]

pro-style (prō-stīl), Archit. —adj. 1. (of a classical temple) having a portico on the front with the columns in front of the antae. —n. 2. a prostyle building or portico. [1890-1700; (adj.) < L. *prostylos* < Gk. *prostylos* with pillars in front, equiv. to *pro-* + *stylos* (n.) < Gk. *prostylos*, n. use of neut. of *prostylos*] —*pro-styl-ic* (prō-stīl-ik), adj.

pro-sy (prō-sē), adj., pro-si-or, pro-si-est. 1. of the nature of or resembling prose. 2. prosaic; dull, tedious, wearisome, or commonplace. [1805-15; *prosa* + -y] —*pro-sy-ly*, adv. —*pro-sy-ness*, n.

pro-syl-lo-gism (prō-sīl-ə-jiz-əm), n. Logic. a syllogism the conclusion of which is used as a premise of another syllogism; any of the syllogisms included in a polysyllogism except the last. Cf. *episylogism*. [1875-85; < ML *prosyllogismus* < Gk. *prosyllogismos*. See *pro-*, -syllogism]

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prot-, var. of *proto-* before a vowel: protamine.

Prot., Protestant.

prot-ac-tin-i-um (prō-tak'tin-ē-əm), n. Chem. a radioactive, metallic element. Symbol: Pa; at. no. 91. Also, *protactinium*. [1915-20; *prot-* + *actinium*]

prot-a-gon-ist (prō-tag'o-nist), n. 1. the leading character, hero, or heroine of a drama or other literary work. 2. a proponent for or advocate of a political cause, social program, etc. 3. the leader or principal person in a movement, cause, etc. 4. the first actor in ancient Greek drama, who played not only the main role, but also other roles when the main character was off-stage. Cf. *deuteragonist*, *tritagonist*. 5. Physiol. agonist. [1665-75; < Gk. *protagonistēs* actor who plays the first part, lit., first combatant, equiv. to *protos* (first) + *agonistes* one who contends for a prize, combatant, actor. See *proto-*, *ANTAGONIST*] —*pro-tag'o-nism*, n.

Pro-tag-o-ras (prō-tag'o-ras), n. c480-c421 B.C., Greek Sophist philosopher. —*Pro-tag'o-ro-an* (prō-tag'o-rō-an), adj. —*Pro-tag'o-ro-an-ism*, n.

prot-a-mine (prō-tā-mēn, prō-tām'in), n. Biochem. any of a group of arginine-rich, strongly basic proteins that are not coagulated by heat, occurring primarily in the sperm of fish. [1870-75; *PROT-* + *AMINE*]

prota-nom-aly (prō-tā-nō-mē-lē), n. Ophthalm. a defect of vision characterized by a diminished response of the retina to red. [1935-40; *PROT-* + *ANOMALY*] —*prot-a-nom-a-lous*, adj.

pro-ta-nom-ia (prō-tā-nō-mē-ā), n. Ophthalm. a defect of vision in which the retina fails to respond to red or green. [1900-05; < NL; see *PROT-*, *AN-*, *-OPIA*] —*pro-ta-nom-i-c* (prō-tā-nō-mē-ik), adj.

pro-ta-sis (prō-tā-sis), n., pl. -ses (-sēz). 1. the clause expressing the condition in a conditional sentence, in English usually beginning with *if*; Cf. *apodosis*. 2. the first part of an ancient drama, in which the characters are introduced and the subject is proposed. Cf. *catastasis*, *catastrophe* (def. 4), *epitasis*. 3. (in Aristotelian logic) a proposition, esp. one used as a premise in a syllogism. [1610-20; < L. *prothesis* introduction in a drama < Gk. *prothesis* proposition, lit., a stretching forward, equiv. to *pro-* + *thesis* a stretching (ta-, verb. s. of *teinain* to stretch + -sis -sis)]

pro-te-an (prō-tē-an, prō-tē-'), adj. 1. readily assuming different forms or characters; extremely variable. 2. (of an actor or actress) versatile; able to play many kinds of roles. 4. (cap.) of, pertaining to, or suggestive of Proteus. [1890-1900; *PROTEUS* + -an] —*pro-te-an-ism*, n.

pro-te-ase (prō-tē-ās, -āz), n. Biochem. any of a group of enzymes that catalyze the hydrolytic degradation of proteins or polypeptides to smaller amino acid polymers. [1900-05; *PROTEIN* + -ase]

protect (pre-tek't), v.t. 1. to defend or guard from attack, invasion, loss, annoyance, insult, etc.; cover or shield from injury or danger. 2. Econ. to guard (the industry or an industry of a nation) from foreign competition by imposing import duties. 3. to provide funds for the payment of (a draft, note, etc.). —v.i. 4. to provide, or be capable of providing, protection: floor wax that protects as well as shines. [1520-30; < L. *protektus*, ptp. of *protegere* to cover in front, equiv. to *pro-* + *tegere* to cover (akin to *tegere*, *thatch*) + -tus ptp. suffix] —*pro-tek-ti-ble*, *pro-tek-ta-ble*, adj. —*pro-tek-ti-bil-i-ty*, *pro-tek-ta-bil-i-ty*, n.

—Syn. 1. screen, shelter. See defend. —Ant. 1. attack.

pro-tek-tant (pre-tek'tant), n. a substance, as a chemical spray, that provides protection, as against insects, frost, rust, etc.; protective agent. [1660-70, for an earlier sense; *PROTECT* + -ant]

pro-tek-tee (prō-tek'tē, prō-tek-tē), n. a person, as a head of state, for whom official protection is provided. [1595-1605; *PROTECT* + -ee]

pro-tek-ting (prō-tek'ting), adj. providing protection or shelter. [1620-30; *PROTECT* + -ing] —*pro-tek-ting-ly*, adv. —*pro-tek-ting-ness*, n.

pro-tec-tion (pre-tek'ti-shən), n. 1. the act of protecting or the state of being protected; preservation from injury or harm. 2. a thing, person, or group that protects: This vaccine is a protection against disease. 3. patronage. 4. Insurance coverage (def. 1). 5. Informal. a. money paid to racketeers for a guarantee against threatened violence. b. bribe money paid to the police, politicians, or other authorities for overlooking criminal activity. 6. Econ. protectionism. 7. a document that assures safety from harm, delay, or the like, for the person, a document given by the U.S. customs authorities to a sailor traveling abroad certifying that the holder is a citizen of the U.S. [1275-1325; ME *protectioun* < L. *protection* (s. of *protektio*) a covering in front. See *protekt*, -ion] —*pro-tek-tion-al*, adj.

—Syn. 1. security, refuge, safety. 2. guard, defense, shield, bulwark. See cover. 3. agent, sponsorship. 7. pass, permit.

pro-tec-tion-ism (pre-tek'ti-shən-iz-əm), n. 1. Econ. the theory, practice, or system of fostering or developing domestic industries by protecting them from foreign competition through duties or quotas imposed on importations. 2. any program, policy, or system of laws that seeks to provide protection for property owners, wildlife,

CONCISE PRONUNCIATION KEY: act, cipe, dare, part; set, equal; if, ice; ox, queer, order, oil, book, better, out; up, urge; child; sing, show, thin; that; sh as in treasure, s = z as in alone, e as in system, i as in easily, o as in gallop, u as in circus; as in fire (fīr), hour (hūr); l and n can serve as syllabic consonants, as in cradle (krād'l) and button (but'n). See the full key inside the front cover.

pro-Par-a-ma', adj.
pro-Pan-a-ma-ni-an, adj., n.
pro-pa-pist, n., adj.
pro-Par-a-guay', adj.
pro-Par-a-guay-an, adj., n.

pro-pa-tri-ot-ic, adj.
pro-pa-tri-ot-ism, n.
pro-pa-tron-age, adj.
pro-pay-ment, adj.
pro-Pe-ru-vi-an, adj., n.

pro-Phil-ip-pine', adj.
pro-Pol-ish, adj.
pro-pol-i-tics, adj.
pro-Par-ti-guere', adj., n.
 pl. -gueres.

pro-Pan-a-ma-ni-an, adj., n.
pro-pa-pist, n., adj.
pro-Par-a-guay', adj.
pro-Par-a-guay-an, adj., n.

pro-pa-tri-ot-ic, adj.
pro-pa-tri-ot-ism, n.
pro-pa-tron-age, adj.
pro-pay-ment, adj.
pro-Pe-ru-vi-an, adj., n.

pro-Phil-ip-pine', adj.
pro-Pol-ish, adj.
pro-pol-i-tics, adj.
pro-Par-ti-guere', adj., n.
 pl. -gueres.

pro-Pan-a-ma-ni-an, adj., n.
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pro-Par-a-guay', adj.
pro-Par-a-guay-an, adj., n.

pro-pa-tri-ot-ic, adj.
pro-pa-tri-ot-ism, n.
pro-pa-tron-age, adj.
pro-pay-ment, adj.
pro-Pe-ru-vi-an, adj., n.

pro-Phil-ip-pine', adj.
pro-Pol-ish, adj.
pro-pol-i-tics, adj.
pro-Par-ti-guere', adj., n.
 pl. -gueres.

pro-Pan-a-ma-ni-an, adj., n.
pro-pa-pist, n., adj.
pro-Par-a-guay', adj.
pro-Par-a-guay-an, adj., n

EXHIBIT 2

United States Patent [19]

Holmberg et al.

[11] Patent Number: 4,820,222
[45] Date of Patent: Apr. 11, 1989

[54] METHOD OF MANUFACTURING FLAT PANEL BACKPLANES INCLUDING IMPROVED TESTING AND YIELDS THEREOF AND DISPLAYS MADE THEREBY

[75] Inventors: Scott H. Holmberg; Richard A. Flasck, both of San Ramon, Calif.

[73] Assignee: Alphasil, Inc., Fremont, Calif.

[21] Appl. No.: 948,224

[22] Filed: Dec. 31, 1986

[51] Int. Cl.⁴ G09G 3/22

[52] U.S. Cl. 445/3; 340/784; 445/24; 437/8

[58] Field of Search 313/500; 340/784; 437/8; 445/3, 24, 25; 29/593

[56] References Cited

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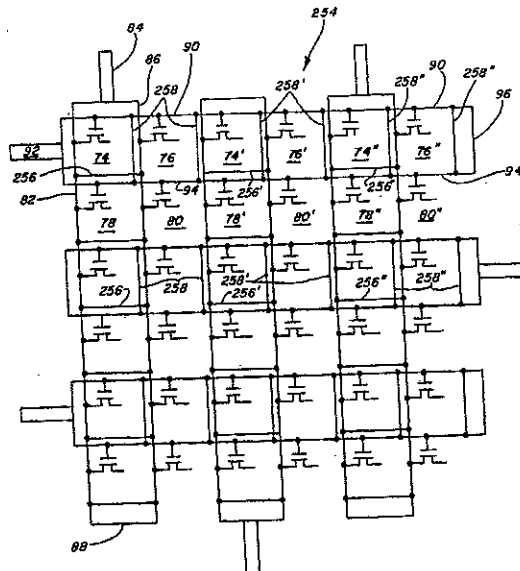
Primary Examiner—Kenneth J. Ramsey
Attorney, Agent, or Firm—Silverman, Cass, Singer & Winburn, Ltd.

[57]

ABSTRACT

Subdivided pixels are provided with interconnected and hence redundant row and column bus lines to reduce fatal defects. The respective redundant row and column lines also can be interconnected between subpixels to further reduce defects. One defective subpixel is generally an acceptable non-fatal defect, since the rest of the subpixels are still operative. The subpixels also can be formed with common row and column bus lines. The pixels or subpixels can be connected in a serial serpentine pattern to test all row or all column bus lines at once. After testing, the serial connections are broken.

31 Claims, 5 Drawing Sheets



U.S. Patent

Apr. 11, 1989

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FIG. 1

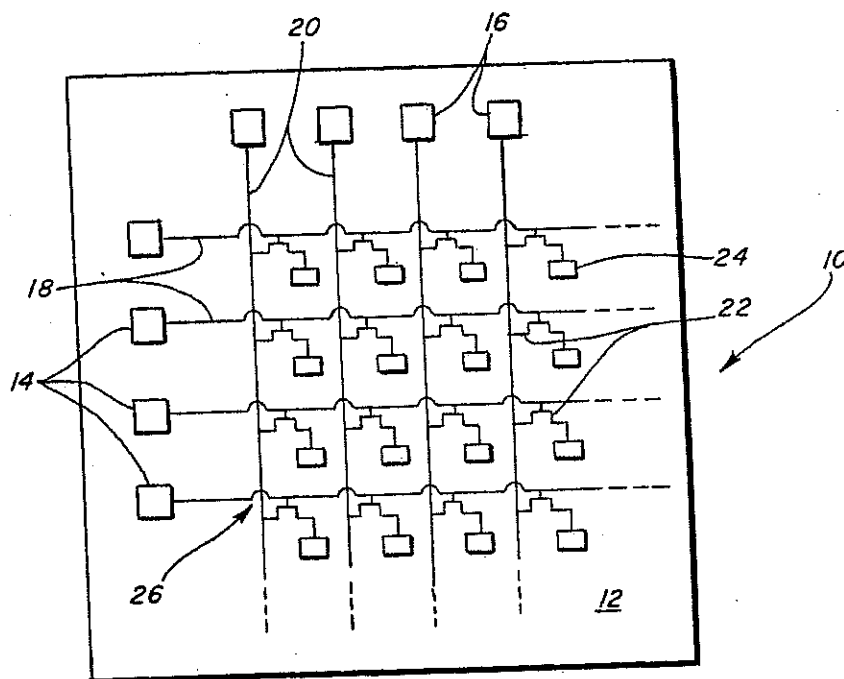


FIG. 2

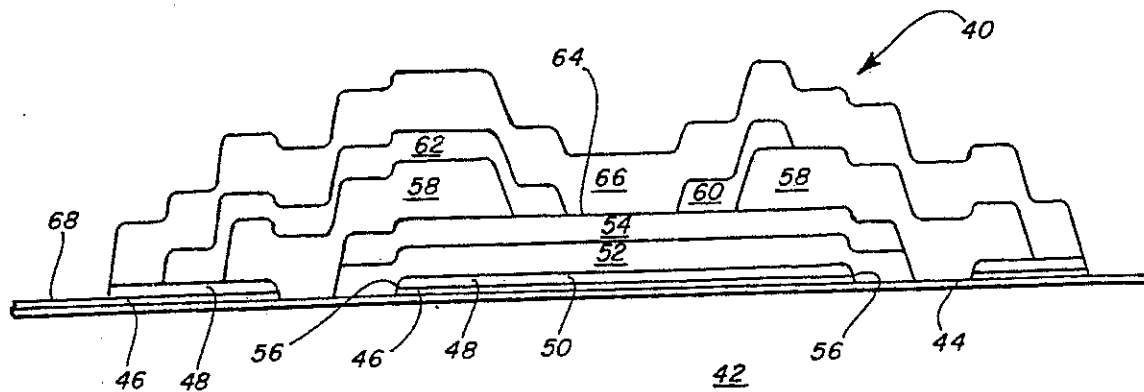
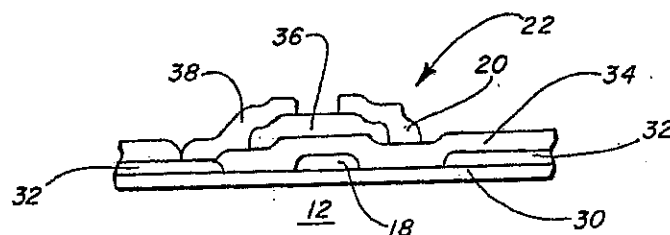


FIG. 3

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FIG. 4

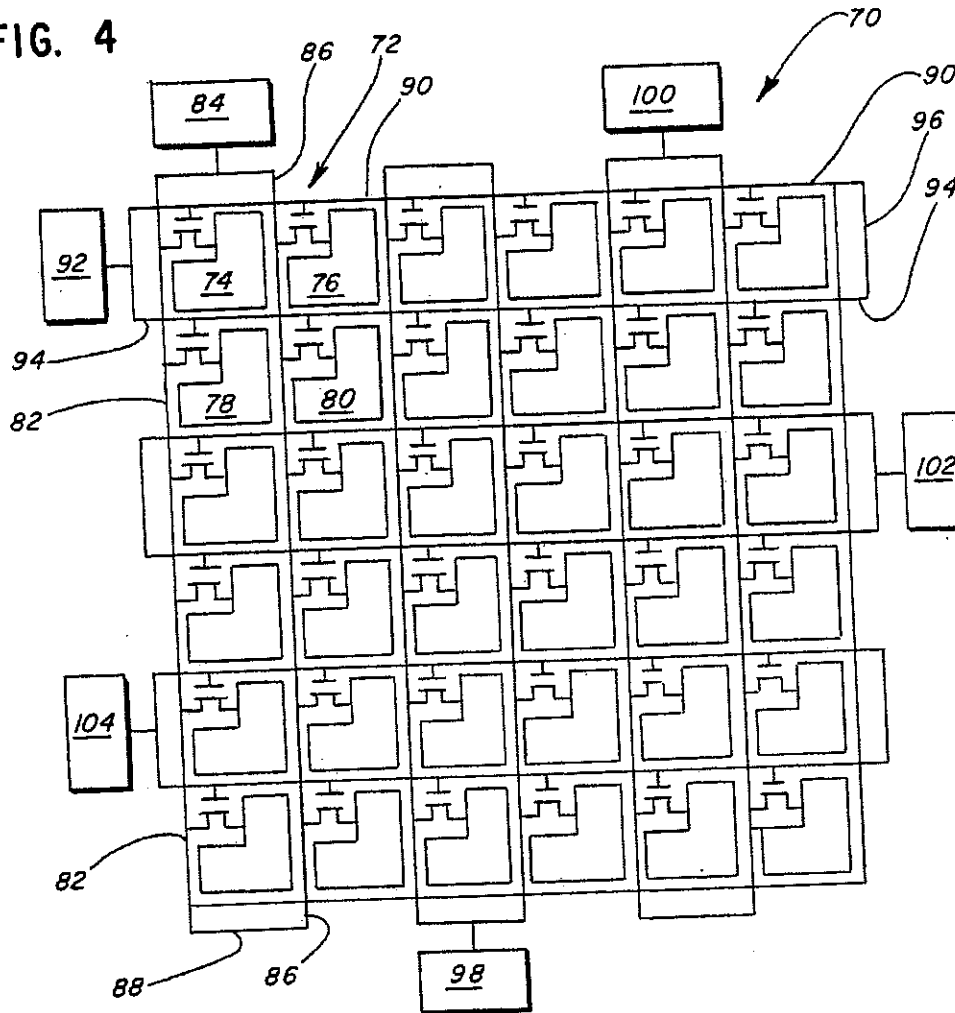
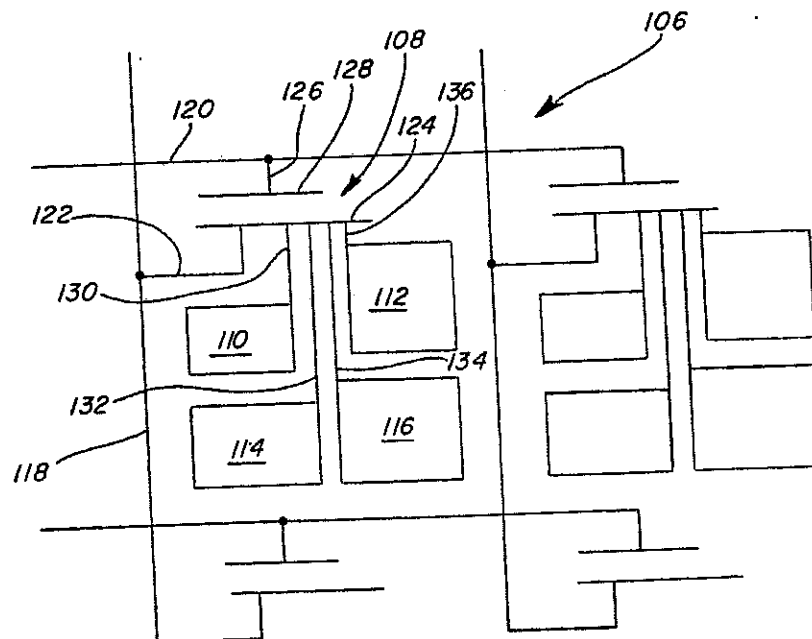


FIG. 5



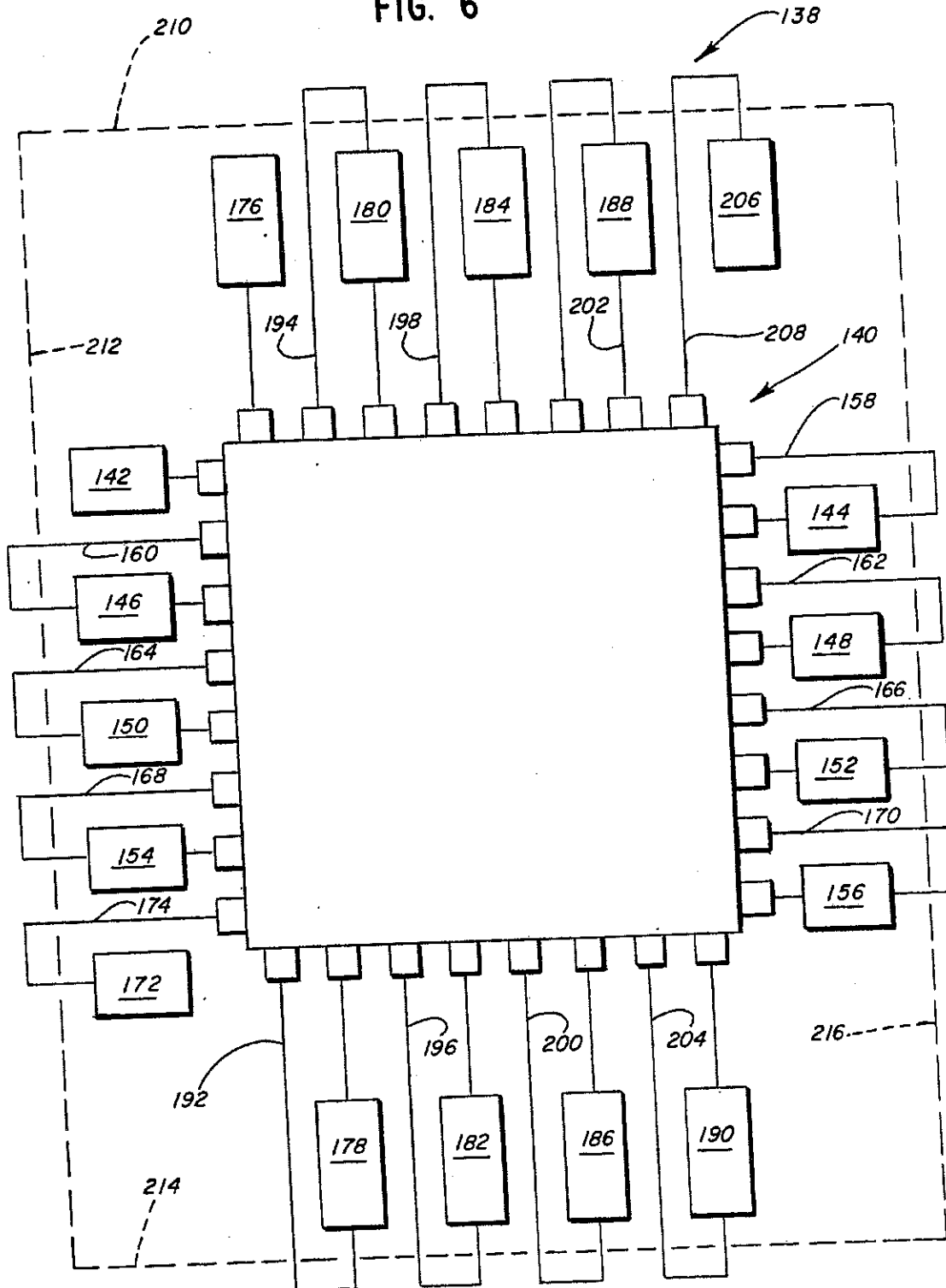
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FIG. 6



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FIG. 7

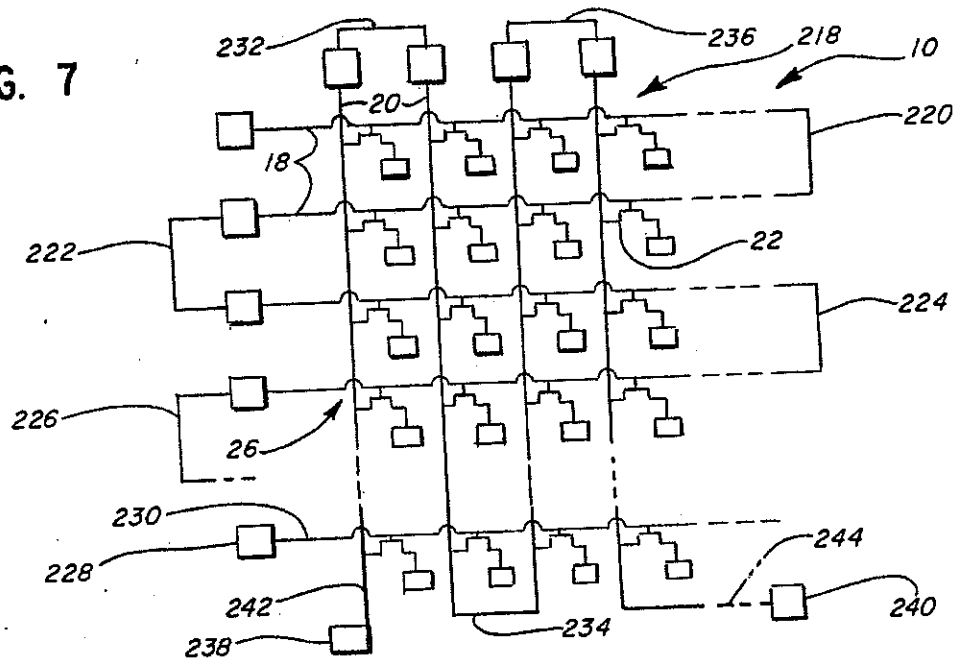
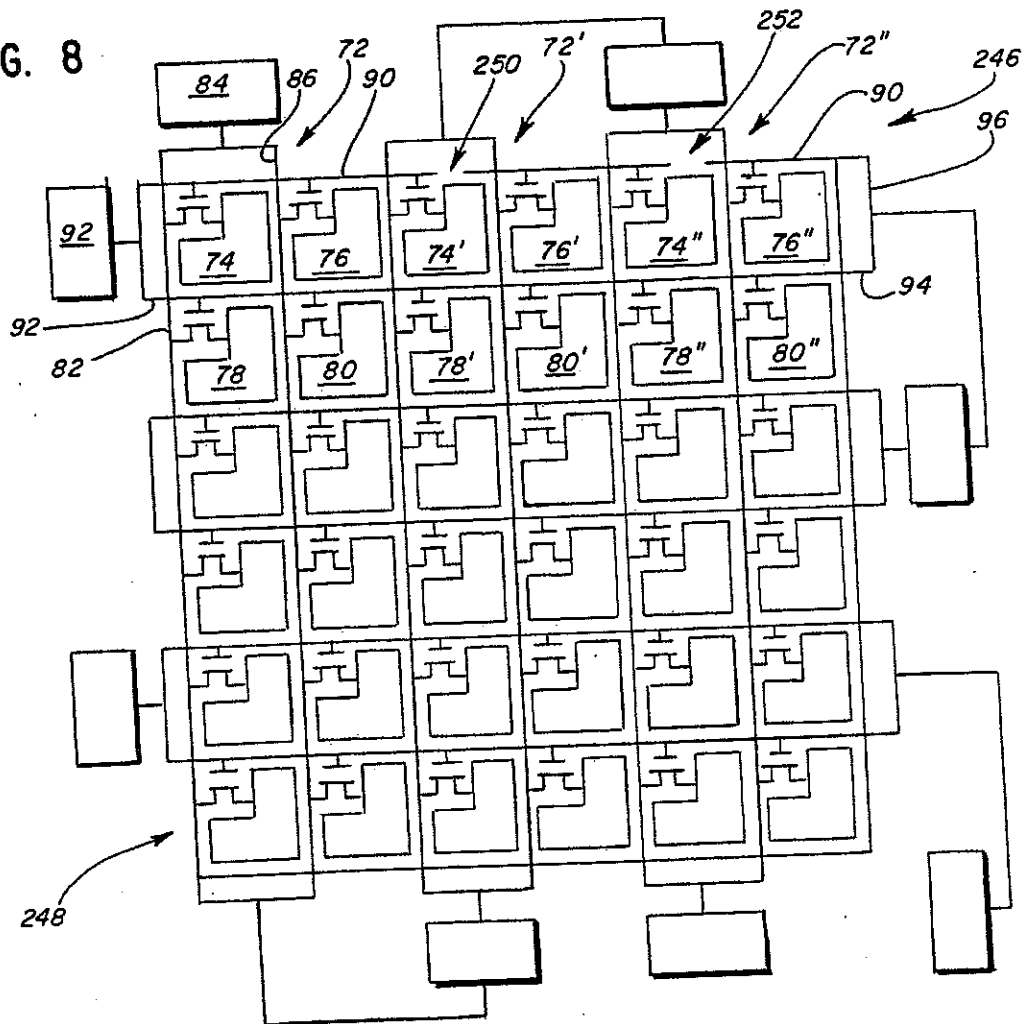


FIG. 8



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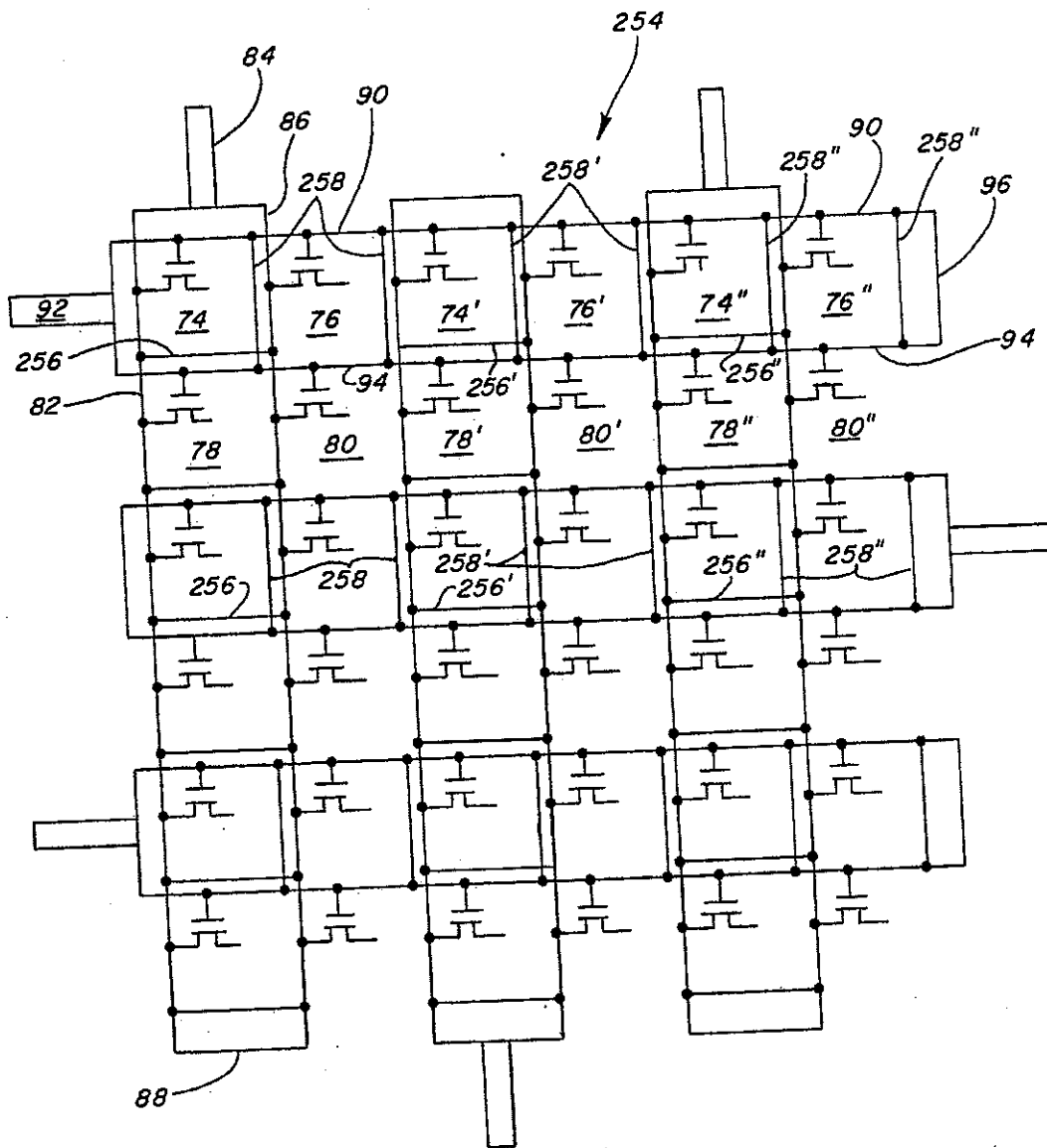


FIG. 9

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METHOD OF MANUFACTURING FLAT PANEL BACKPLANES INCLUDING IMPROVED TESTING AND YIELDS THEREOF AND DISPLAYS MADE THEREBY

BACKGROUND OF THE INVENTION

The present invention pertains to improved flat panel displays and methods of making and testing the displays. More particularly, the present invention is directed to methods of increasing the manufacturing yields of flat panel display backplanes and the displays made therefrom.

In recent years there has been growing interest in flat panel displays, such as those which employ liquid crystals, electrochromic or electroluminescence, as replacements for conventional cathode ray tubes (CRT). The flat panel displays promise lighter weight, less bulk and substantially lower power consumption than CRT's. Also, as a consequence of their mode of operation, CRT's nearly always suffer from some distortion. The CRT functions by projecting an electron beam onto a phosphor-coated screen. The beam will cause the spot on which it is focused to glow with an intensity proportional to the intensity of the beam. The display is created by the constantly moving beam causing different spots on the screen to glow with different intensities. Because the electron beam travels a further distance from its stationary source to the edge of the screen than it does to the middle, the beam strikes various points on the screen at different angles with resulting variation in spot size and shape (i.e. distortion).

Flat panel displays are manufactured to be substantially free of such distortion. In the manufacture of flat panel displays the circuit elements are deposited and patterned, generally by photolithography, on a substrate, such as glass. The elements are deposited and etched in stages to build a device having a matrix of perpendicular rows and columns of circuit control lines with a pixel contact and control element between the control line rows and columns. The pixel contact has a medium thereon which is a substance that either glows (active) or changes its response to ambient light (passive) when a threshold voltage is applied across the medium control element. The medium can be a liquid crystal, electroluminescent or electrochromic materials such as zinc sulfide, a gas plasma of, for example, neon and argon, a dichloroic dye, or such other appropriate material or device as will luminesce or otherwise change optical properties in response to the application of voltage thereto. Light is generated or other optical changes occur in the medium in response to the proper voltage applied thereto. Each optically active medium is generally referred to as a picture element or "pixel".

The circuitry for a flat panel display is generally designed such that the flat panel timeshares, or multiplexes, digital circuits to feed signals to one row and column control line of the pixels at a time. Generally one driving circuit is used for each row or column control line. In this way a subthreshold voltage can be fed to an entire row containing hundreds of thousands of pixels, keeping them all dark or inactive. Then a small additional voltage can be supplied selectively to particular columns to cause selected pixels to light up or change optical properties. The pixels can be made to glow brighter by applying a larger voltage or current of a longer pulse of voltage or current. Utilizing liquid crystal displays (LCD's) with twisted nematic active

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material, the display is substantially transparent when not activated and becomes light absorbing when activated. Thus, the image is created on the display by sequentially activating the pixels, row by row, across the display. The geometric distortion described above with respect to CRT's is not a factor in flat panel displays since each pixel sees essentially the same voltage or current.

One of the major problems that arises with respect to the prior art method of manufacture of backplanes for active matrix displays (e.g. those employing thin film transistors at each pixel) is that they generally suffer production yield problems similar to those of integrated circuits. That is, the yields of backplanes produced are generally not 100% and the yield (percentage of backplanes with no defects) can be 0% in a worst case. High quality displays will not tolerate any defective pixel transistors or other components. Also, larger size displays are generally more desirable than smaller size displays. Thus, a manufacturer is faced with the dilemma of preferring to manufacture larger displays, but having to discard the entire product if even one pixel is defective. In other words, the manufacturer suffers a radically increased manufacturing cost per unit resulting from decreasing usable product yield.

These problems of increased cost and decreased yield are dramatically improved in the present invention by providing methods of manufacturing display backplanes and the resulting displays with a greatly reduced number of fatal defects.

SUMMARY OF THE INVENTION

There is provided improved methods of manufacturing backplanes and the resulting flat panel displays to greatly increase the manufacturing yield, decrease manufacturing costs and decrease the number of fatal display defects.

These improvements are accomplished by subdividing each of the backplanes and hence display pixels into two or more subpixels. Each subpixel is formed with its own row (gate) line and column (source) bus line. Each subpixel pair of bus row lines and each pair of bus column lines are connected at the opposite sides of the display to provide redundant bus row lines and bus column lines. A break in the row or column bus line therefore will not affect the operation of the display, because the pixel will receive current from the other interconnected end of the row or column bus line. Further, by providing subpixels, a defective active device at a subpixel will result in less than the whole pixel being defective and hence can be an acceptable nonfatal defect increasing the display yields. Subpixels also can be formed with a common row and a common column bus line.

The cost of manufacturing the display backplanes and hence the displays also can be reduced by serial loop testing of the row and column bus lines during manufacture. Each of the row and column bus lines is serially interconnected in a serpentine fashion at the opposite edges of the display. This allows all the row and all the column bus lines to be tested merely by contacting the two free ends of each of the serially interconnected row and column bus lines. Further, by applying the proper voltage to the ends of both the row and column bus lines, all the pixels or subpixels will be activated to provide one whole display test of all the pixels or subpixels at once. After final testing, the row and bus col-

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umn line interconnections are broken to complete the display.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view schematic representation of an active matrix display backplane made by a prior art method;

FIG. 2 is a cross-section of one transistor of the prior art backplane which could be utilized with the present invention;

FIG. 3 is a cross-section of one transistor which could be utilized with the present invention;

FIG. 4 is a plan view schematic representation of one embodiment of a subpixel matrix display of the present invention;

FIG. 5 is a plan view schematic representation of another embodiment of a subpixel matrix display of the present invention;

FIG. 6 is a plan view schematic representation of one embodiment of serial serpentine testing of the subpixel row and column bus lines in accordance with the present invention;

FIG. 7 is a plan schematic view of serial serpentine testing of conventional row and column bus lines in accordance with the present invention;

FIG. 8 is a plan view schematic of the subpixel matrix display of FIG. 4 with several row and column bus line defects or breaks therein; and

FIG. 9 is a plan view schematic of a subpixel matrix display of the invention similar to FIG. 8 with row and column bus line interconnections to avoid fatal defects caused by greater than one break in a particular row or bus column line.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now more particularly to FIG. 1, there is shown a schematic representation of an active matrix flat panel display device 10 made in accordance with conventional photolithographic techniques. One such device 10 and the manufacture thereof is more fully described in Application of Amorphous Silicon Field Effect Transistors in Addressable Liquid Crystal Display Panels, A. J. Snell, et al., *Applied Physics*, No. 24, p. 357, 1981. The device 10 includes a substrate 12, sets of contact pads 14 and 16, sets of control or bus lines 18 and 20, and, in this particular example of the prior art, transistors 22 and pixel back contacts 24.

The substrate 12 commonly employed in these devices is formed from glass. The control lines 18 and 20 are organized into a matrix of rows 18 and columns 20. The control line rows 18 in this device 10 serve as gate electrodes and the control line columns 20 as source connections. One contact pad 14 is connected to one end of each of the row control lines 18. One contact pad 16 is connected to one end of each of the column control lines 20. The display drive control (not shown) is connected to the sets of pads 14 and 16.

At each matrix crossover point 26, where a row line 18 and a column line 20 cross, a switching element, transistor 22 is formed to connect the row line 18 and column line 20 to the pixel back contacts 24. The active medium is deposited at least on the contacts 24 which will optically change properties in response to the combined voltages or currents in the respective crossover point 26 formed by the row 18 and column 20. The active medium at a given crossover point 26 will appear as a square or dot in the overall checkerboard type

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matrix of the display 10. The actual size of the transistors 22 and the contacts 24 are not now drawn to scale, but are shown schematically for illustration only.

It should be noted that theoretically there is no limit on the number of rows 18 and columns 20 that can be employed, only a portion of which are illustrated in FIG. 1. Therefore, there is also no theoretical limit on the outside dimensions of such a device 10. However, the present state of the lithographic art places a practical limit on the outside dimensions of these devices. The present alignment techniques generally allow high resolution display devices to be manufactured approximately five inches on a side 28, although improved techniques of up to fourteen inches on a side has been demonstrated.

The problem encountered by the prior art method of manufacture is that if the array of device 10 contains any defective pixel transistors 22 or other circuit elements causing a pixel to be inoperative, it must be discarded.

Referring in detail to FIG. 2, several problems occur when the switching element, transistor 22 is manufactured. The substrate 12 is a substantial portion of the backplane cost and hence an inexpensive soda-lime glass is generally utilized. It has been demonstrated by liquid crystal display manufacturers that the high sodium concentration can poison the liquid crystal material by diffusing through the overlying ITO layer and hence an SiO₂ suppression layer 30 is generally formed on the substrate 12. There are some high quality low sodium types of substrates available, which would not need the suppression layer 30. An ITO layer 32 is formed and etched to provide an ITO free area on which the gate 18 is deposited. Following the deposition of the gate 18, a gate insulator layer 34 is deposited. Although a smooth uniform coverage of the gate 18 by the insulator 34 is illustrated, in production the gate 18 has or can have sharp edges which lead to pin holes or thinning of the insulator 34 at the gate edges. The source and drain metals can short to the gate 18. The thinning or pin holes produce transistors 22, which if operative, do not have uniform operating characteristics and hence the backplane is worthless.

One attempt to solve this problem, is to make the gate 18 very thin, but the resistivity is then too high to make the large arrays necessary for the backplane. A second attempt to solve the problem is to make the gate insulator 34 very thick, but this decreases the gain of the transistor 22 and is also self defeating.

An amorphous silicon layer 36 is then deposited, with the source 20 and a drain 38 deposited thereover. A passivating layer (not shown) would be deposited over the completed structure to complete the transistor 22. During operation the activation of the source 20 and the gate 18 couples power through the silicon alloy 36 to the drain and hence to the contact pad 24 formed by the ITO layer 32.

Referring now to FIG. 3, there is shown a schematic representation of one embodiment of a transistor 40 which can be utilized with the present invention. The transistor is more fully disclosed in U.S. Pat. No. 4,545,112 and U.S. Ser. No. 493,523, which are incorporated herein by reference.

A glass substrate 42 includes a barrier SiO₂ layer 44 thereon. As above mentioned, a low sodium glass substrate, such as Corning 7059 glass, could be utilized, and hence the barrier layer 44 can be eliminated. The detailed deposition steps are described in the above-

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referenced patent and application. An ITO layer 46 is deposited and then a refractory metal layer 48 is deposited on the ITO layer 46.

The layers 46 and 48 are etched to form a gate electrode 50. A gate insulator 52 and a semiconductor material 54 are sequentially deposited over the gate 50. The material 54 preferably is an amorphous silicon alloy. To avoid the possibility of any gate to source or drain shorts at gate edges 56, a dielectric 58 is deposited over the gate 55, the gate insulator 52 and the semiconductor 54. The dielectric 58 is deposited to a sufficient thickness to ensure that no shorts or thin spots are formed between the edges 56 of the gate 50 and a source 60 and a drain 62 deposited thereover.

The dielectric 58 is etched away only on a substantially planar central region 64 of the semiconductor layer 54. This insures uniform operating characteristics for the transistors 40 in the backplane array. A passivating layer 66 is deposited over the whole structure to complete the structure of the transistor 40.

During all of the transistor processing steps, the refractory metal layer 48 remains over a pixel contact pad 68 upon which the active material of the pixel is deposited. As a final step, before the active medium (not shown) is added to the backplane to complete the display, the refractory metal is etched off of the pixel pad 68 leaving the ITO layer 46 exposed after all the processing has been completed.

Referring now to FIG. 4, a subpixel matrix display of the present invention is designated generally by the reference numeral 70. The subpixel matrix display 70 is illustrated as having each pixel subdivided into four subpixels, but the pixels could be subdivided into numerous other configurations such as two subpixels, two by four or six subpixels or in three subpixels for color applications. Each pixel 72 is subdivided into four subpixels 74, 76, 78 and 80 (only one pixel 72 is so numbered for illustration). As previously stated, the number of pixels is merely shown for illustration purposes and the display 70 could contain any desired number and configuration, square or rectangular.

A column (source) line or bus 82 connects the subpixels 74 and 78 and all other column subpixel pairs in one-half of each of the pixels to a column or source contact pad 84 at one edge of the display 70. A second column (source) line or bus 86 connects the subpixels 76 and 80 and all other column subpixel pairs in the second half of each of the pixels to the column or source contact pad 84. The bus lines 82 and 86 are interconnected (shorted) at or before the pad 84 and are interconnected (shorted) at the opposite ends by a line or short 88.

A row (gate) line or bus 90 connects the subpixels 74 and 76 and all other row subpixel pairs in one-half of each of the pixels to a row (gate) pad 92. A second row (gate) line or bus 94 connects the subpixels 78 and 80 and all other row subpixel pairs in one-half of each of the pixels to the row pad 92. The bus lines 90 and 94 are interconnected (shorted) at or before the pad 92 and are interconnected (shorted) at the opposite ends by a line or short 96.

In a like manner, each of the other subpixel pairs are connected in columns to respective column (source) pads 98 and 100, etc. The pads 84, 98 and 100 are illustrated as being on opposite sides of the display to provide additional connecting space for the pads, however, they also could all be on one side as in the display 10.

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Each of the other subpixel pairs also are connected in rows to respective row (gate) pads 102 and 104, etc.

The pixel 72 then is divided into four subpixels 74, 76, 78 and 80 which allows for one of the subpixels to be defective, such as the subpixel 74, without causing a fatal defect, since the remaining three subpixels 76, 78 and 80 remain operative. In prior devices, the pixel 72 would be totally defective and hence the display 70 would be inoperable.

Further, one often fatal display defect is caused by a defect or open in one of the row or column bus lines which would cause the whole row or column to be out, again resulting in an inoperative display 70. With the respective subpixel pairs of row and column bus lines interconnected, however, an open in a bus line will at most cause one subpixel to be inoperative. An open in one or more of the bus lines between the subpixels will result in no defects, since the current is supplied from the opposite shorted end of the row or column bus line. Thus, the display 70 in effect has redundant row and column bus lines.

Referring to FIG. 5, a second embodiment of a subpixel matrix display of the present invention is designated generally by the reference numeral 106. Again, a pixel 108 is subdivided into a plurality of subpixels 110, 112, 114 and 116. In this embodiment, each of the subpixels 110, 112, 114 and 116 has a common column (source) line or bus 118 and a common row (gate) line or bus 120. The column bus line 118 is coupled by a source line 122 to a line 124, which is a schematic representation of a common source electrode. The row bus line 120 is coupled (schematically) by a line 126 to a line 128 which is a schematic representation of a gate electrode. Each of the subpixels 110, 112, 114 and 116 is coupled by a separate respective drain line 130, 132, 134 and 136 to the (schematic) common source electrode 124. Since the drain lines 130, 132, 134 and 136 are small and formed close to one another to utilize the least space, a short in one of the lines, such as the drain line 130 causes only the subpixel 110 to be defective.

A flat panel backplane testing configuration is generally designated by the numeral 138 in FIG. 6. A flat panel backplane configuration 140 having subpixels similar to the display 70 of FIG. 4 includes a plurality of interconnected row (gate) lines or buses which are connected as described above to a plurality of row (gate) pads 142, 144, 146, 148, 150, 152, 154 and 156.

Additionally, each of the row pads 142, 144, 146, 148, 150, 152, 154 and 156 and hence each of the row (gate) lines or buses is interconnected in a serpentine fashion by respective lines or shorts 158, 160, 162, 164, 166, 168 and 170. In addition, to allow the testing of the last pair of row lines from the row pad 156, an additional or test row pad 172 is added to the test configuration 138, which is coupled to the last pair of row bus lines by a line 174.

Each of a pair of a plurality of interconnected column (source) lines or buses is connected to a respective column (source) pad 176, 178, 180, 182, 184, 186, 188 and 190 as described above. As with the row bus lines and pads, each column pad 176, 178, 180, 182, 184, 186, 188 and 190 is interconnected in a serpentine fashion by respective lines or shorts 192, 194, 196, 198, 200, 202 and 204. Again, to test the last pair of column bus lines, an additional or test column pad 206 is added to the test configuration 138, which is coupled to the last pair of column bus lines by a line 208.

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As soon as the row bus lines (presuming the row bus lines are deposited first) are formed, all of the row bus lines can be tested merely by contacting two test points, the pads 142 and 172. In a like manner, the column bus lines can be tested simultaneously by contacting the two pads 176 and 206. The tests can be repeated as desired during the manufacturing process and appropriate repairs or termination of the manufacturing process can occur to reduce the manufacturing costs and to increase the yield of the completed display.

If the display is an inactive matrix without transistors or other active devices, then once the row and column bus lines have been tested as having continuity, then the serpentine interconnections are opened or broken to complete or allow completion of the display backplane. Preferably, especially where the devices are formed on glass, the interconnecting lines 158, 160, etc. and 192, 194, etc. extend beyond their respective pads, such that four scribe lines 210, 212, 214 and 216 intersecting all of the connecting lines can be formed. The glass substrate then is broken off along each of the scribe lines 210, 212, 214 and 216 to terminate the test interconnections.

Where the subpixel display device 140 includes active devices, such as the transistors previously described, then the transistors also will be tested prior to terminating the interconnections. Further, if desired, the liquid crystal medium can be added and the whole display can be tested at once to see if all the pixels of the whole display 140 are operable prior to terminating the connections. In this case, one or both row pads 142 and 172 are contacted with an appropriate row or gate activation voltage.

In a like manner, one or both column pads 176 and 206 are contacted with an appropriate column or source activation voltage. Also, the backplane contact (not illustrated) is contacted with an appropriate activation voltage, which will activate all of the pixels for a visual test of the display device 140.

Referring to FIG. 7, the prior art device 10 (FIG. 1) is illustrated having a test configuration 218. The row bus lines 18 are interconnected in a serpentine fashion by a plurality of connecting lines 220, 222, 224 and 226 (partially shown). Depending upon the number of bus lines, the device 10 may not need an additional test pad, since the device ends in a pad 228 on the last row bus line 230. In a like manner, the column bus lines are interconnected in a serpentine fashion by a plurality of connecting lines 232, 234 and 236. If desired, or the configuration requires, a pair of column test pads 238 and 240 with respective connecting lines 242 and 244 are utilized to test the display 10 as described with respect to FIG. 6, prior to terminating or removing the connecting lines. Generally, the device 10 would be configured with the column pads all on the same side as illustrated for the row pads.

Referring to FIG. 8, a test configuration 246 with a subpixel display 248 is best illustrated, which is similar to the display 70 of FIG. 4, with the serpentine test configuration of FIG. 6. Like numerals for the like parts from those described in FIG. 4, are utilized where appropriate. As described before, the redundant row bus lines 90 and 94 will provide the operating current to all the subpixels 74, 76, 74', 76', etc. if a single break or defect 250 occurs in one of the lines 90. In that case the row bus lines for the subpixels 74, 76 and 74' are fed from the pad 92 on one end of the bus line 90, while the subpixels 76', 74'' and 76'' are fed via the pad 92, the bus line 94 across the short 96 and via the other end of the

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bus line 90. If, however, a second break 252 occurs in the same bus line 90, then no current will be fed to the subpixels 76' and 74'', which then are isolated. Two or more adjacent subpixels being inoperative generally would be a fatal defect and the redundant row bus lines 90 and 94 then would not be sufficient to save the display 248. In a like manner, two or more breaks in any of the row or column bus lines or pairs of bus lines generally will render the display inoperative.

To avoid the fatal defect of the multiple open lines another redundant display configuration is designated generally by the numeral 254 in FIG. 9. The redundant row and column bus lines are further interconnected in the display 254 at each subpixel to avoid the fatal defect illustrated in FIG. 8.

The display 254 is illustrated only with the bus line and interconnection patterns without the subpixels for clarity. Each pair of the column bus lines 82 and 86 are additionally interconnected between each of the subpixels 74, 78, etc. by respective lines or shorts 256, 256' and 256''. In a like manner, each pair of the row bus lines 90 and 94 are interconnected between each of the subpixels 74, 76, etc. by respective lines or shorts 258.

With the additional interconnections 256 and 258, the previously fatal double open defects 250 and 252 do not cause the loss of any subpixels. The subpixels 76' and 74'' now are fed via the bus line 94 and the short connecting line 258'. Therefore, the display 254 does not have any subpixel defects. Further, although both the row bus lines and the column bus lines have been illustrated as being interconnected between each subpixel, only one of the row or the column bus line sets might be shorted to limit the loss of active pixel display area.

Modification and variations of the present invention are possible in light of the above teachings. The transistors 22 or other types of two or three terminal switching devices can be utilized with the invention. The amorphous silicon alloy semiconductor material 54, could be any of numerous types of materials such as CdSe or GaAs materials. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

What is claimed and desired to be secured by Letters Patent of the United States is:

1. A method of manufacturing matrix display backplanes and displays therefrom, comprising:

providing a substrate;
providing a pattern of pixels on said substrate; and
providing a plurality of sets of intersecting pixel activation bus lines and coupling each said pixel to a pair of said sets of intersecting bus lines to provide each pixel with a redundant pair of activation bus lines, including connecting each of said pixels to one of its redundant pair of activation bus lines and interconnecting each end of said redundant pair of activation bus lines to one another to provide said redundancy and dividing each pixel into a plurality of subpixels and connecting each of said subpixels to one of its redundant pair of activation bus lines through an active device, independent of any other pixel activation bus lines.

2. The method as defined in claim 1 including interconnecting each of said redundant pair of activation bus lines between each of said pixels.

3. The method as defined in claim 1 including providing a redundant pair of row activation bus lines and a

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redundant pair of column activation bus lines for each of said pixels.

4. The method as defined in claim 3 including interconnecting at least one pair of said row and column lines between each of said pixels.

5. A display having dual bus lines, comprising:

a substrate;

a pattern of pixels formed on said substrate; and

a plurality of sets of intersecting pixel activation bus lines formed on said substrate and each said pixel coupled to a pair of said sets of intersecting bus lines to provide each pixel with a redundant pair of activation bus lines, including each of said pixels connected to one of its redundant pair of activation bus lines and each end of said redundant pair of activation bus lines interconnected to one another to provide said redundancy and each pixel divided into a plurality of subpixels and each of said subpixels connected to one of its redundant pair of activation bus lines through an active device, independent of any other pixel activation bus lines.

6. The display as defined in claim 5 including each of said redundant pair of activation bus lines interconnected between each of said pixels.

7. The display as defined in claim 5 including a redundant pair of row activation bus lines and a redundant pair of column activation bus lines connected to each of said pixels.

8. The display as defined in claim 7 including at least one pair of said row and column lines interconnected between each of said pixels.

9. A method of manufacturing matrix display backplanes and displays therefrom, comprising:

providing a substrate;

providing a pattern of pixels on said substrate;

providing a plurality of sets of intersecting pixel activation bus lines and coupling each said pixel to at least one of said sets of intersecting bus lines to provide each pixel with a set of activation bus lines;

forming said activation bus lines substantially orthogonal to one another in a plurality of rows and a plurality of columns of bus lines;

interconnecting opposite ends of each of said plurality of row bus lines in a serpentine fashion to serially connect substantially all of said row bus lines to one another;

interconnecting opposite ends of each of said plurality of column bus lines in a serpentine fashion to serially connect substantially all of said column bus lines to one another;

testing the continuity of substantially all of said plurality of row and column bus lines by contacting only two test points on each of said interconnected row and column bus lines as the backplanes are being manufactured; and

terminating substantially all of said interconnections after said bus lines are tested as having continuity to complete the manufacture of the backplanes and displays therefrom.

10. The method as defined in claim 9 including providing a plurality of sets of intersecting pixel activation bus lines and coupling each said pixel to a pair of said sets of intersecting bus lines to provide each pixel with a redundant pair of activation bus lines and interconnecting opposite ends of each respective pair of said plurality of row and column bus lines to test the continuity of said sets of row and column bus lines.

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11. The method as defined in claim 10 including connecting each of said pixels to one of its redundant pair of activation bus lines and interconnecting each end of said redundant pair of activation bus lines to one another to provide said redundancy.

12. The method as defined in claim 11 including dividing each pixel into a plurality of subpixels and connecting each of said subpixels to one of its redundant pair of activation bus lines.

13. The method as defined in claim 12 including interconnecting at least one pair of said row and column lines between each of said pixels.

14. A display backplane having interconnections, comprising

a substrate;

a pattern of pixels formed on said substrate;

a plurality of sets of intersecting pixel activation lines formed on said substrate and each said pixel coupled to at least one of said sets of intersecting lines by an active device to provide each pixel with a set of activation lines;

said activation lines formed substantially orthogonal to one another in a plurality of rows and a plurality of columns of lines;

opposite ends of each of said plurality of row lines interconnected in a serpentine fashion to serially connect substantially all of said row lines to one another;

opposite ends of each of said plurality of column bus lines interconnected in a serpentine fashion to serially connect substantially all of said column bus lines to one another; and

a pair of test points on each of said row and said column bus lines.

15. The backplane as defined in claim 14 including a plurality of sets of intersecting pixel activation bus lines, each said pixel coupled to a pair of said sets of intersecting bus lines to provide each pixel with a redundant pair of activation bus lines and opposite ends of each respective pair of said plurality of row and column bus lines interconnected.

16. The backplane as defined in claim 15 including each of said pixels connected to one of its redundant pair of activation bus lines and each end of said redundant pair of activation bus lines interconnected to one another to provide said redundancy.

17. The backplane as defined in claim 16 including each pixel divided into a plurality of subpixels and each of said subpixels connected by an active device to one of its redundant pair of activation bus lines.

18. The backplane as defined in claim 17 including at least one pair of said row and column lines interconnected between each of said pixels.

19. A method of manufacturing matrix display backplanes and displays therefrom, comprising:

providing a substrate;

providing a pattern of pixels on said substrate;

subdividing each of said pixels into at least two subpixels; and

providing a plurality of sets of intersecting subpixel activation bus lines and coupling each said subpixel to at least one of said sets of intersecting bus lines to provide each subpixel with a set of activation bus lines through an active device, independent of any other pixel activation bus lines.

20. The method as defined in claim 19 including connecting each of said subpixels to one of its redundant pair of activation bus lines and interconnecting each end

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of said redundant pair of activation bus lines to one another to provide said redundancy.

21. The method as defined in claim 20 including interconnecting each of said redundant pair of activation bus lines between each of said subpixels.

22. The method as defined in claim 24 including interconnecting opposite ends of each of said plurality of row bus lines in a serpentine fashion to serially connect substantially all of said row bus lines to one another; interconnecting opposite ends of each of said plurality of column bus lines in a serpentine fashion to serially connect substantially all of said column bus lines to one another;

testing the continuity of substantially all of said plurality of row and column bus lines by contacting only two test points on each of said interconnected row and column bus lines as the backplanes are being manufactured; and

terminating substantially all of said interconnections after said bus lines are tested as having continuity to complete the manufacture of the backplanes and displays therefrom.

23. The method as defined in claim 22 including testing all of said subpixels by contacting said two row and said two column bus line test points.

24. The method as defined in claim 19 including providing a redundant pair of row activation bus lines and a redundant pair of column activation bus lines for each of said subpixels.

25. The method as defined in claim 24 including interconnecting at least one pair of said row and column lines between each of said subpixels.

26. A display backplane having subpixels, comprising:

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a substrate;

a pattern of pixels formed on said substrate; each of said pixels subdivided into at least two subpixels; and

a plurality of sets of intersecting pixel activation bus lines formed on said substrate and each said subpixel coupled to at least one of said sets of intersecting bus lines to provide each subpixel with a set of activation bus lines through an active device, independent of any other pixel activation bus lines.

27. The display as defined in claim 26 including each of said subpixels connected to one of its redundant pair of activation bus lines and each end of said redundant pair of activation bus lines interconnected to one another to provide said redundancy.

28. The display as defined in claim 27 including each of said redundant pair of activation bus lines interconnected between each of said subpixels.

29. The display as defined in claim 27 including opposite ends of each of said plurality of row bus lines interconnected in a serpentine fashion to serially connect substantially all of said row bus lines to one another; and opposite ends of each of said plurality of column bus lines interconnected in a serpentine fashion to serially connect substantially all of said column bus lines to one another.

30. The display as defined in claim 26 including a redundant pair of row activation bus lines and a redundant pair of column activation bus lines connected to each of said subpixels.

31. The display as defined in claim 30 including at least one pair of said row and column lines interconnected between each of said subpixels.

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EXHIBIT 3

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

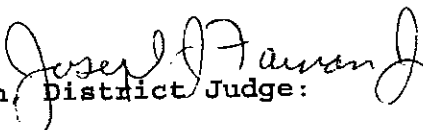
LG. PHILIPS LCD CO. LTD, :
 :
 Plaintiff, :
 :
 v. : Civil Action No. 05-292-JJF
 :
 TATUNG COMPANY, TATUNG COMPANY :
 OF AMERICA, INC., CHUNGWHA :
 PICTURE TUBES LTD., and :
 VIEWSONIC CORP., :
 :
 Defendants. :

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MEMORANDUM OPINION

June 13, 2006
Wilmington, Delaware


Farnan, District Judge:

Plaintiff L.G. Philips LCD Co., LTD ("LPL") filed this patent infringement action against Defendants Tatung Company, Tatung Company of America, Inc., Chungwha Picture Tubes, LTD., and ViewSonic Corporation (collectively "CPT"). LPL alleges that CPT has infringed U.S. Patent No. 5,019,002 ("the '002 patent"). LPL's Complaint (D.I. 1) also alleges infringement of U.S. Patent No. 6,738,121 ("the '121 patent"), but LPL has withdrawn all claims relating to that patent. (D.I. 180.) Presently before the Court is the claim construction dispute of the parties. The parties briefed their respective positions, and the Court held a Markman hearing on March 20, 2006. This Memorandum Opinion provides the Court's construction of the claim terms and phrases disputed by the parties.

BACKGROUND

The Patent at issue in this lawsuit relates to flat panel, display screens and methods of manufacturing them that include electrostatic discharge guard rings to protect the active elements of the display from electrostatic discharge during and after manufacturing. In their briefing and at the Markman hearing, the parties disputed twenty-six terms and phrases from the claims of both the '002 patent and the '121 patent. By its Order dated March 22, 2006 (D.I. 155), the Court ordered the parties to select a reduced number of terms and phrases to be

construed by the Court. The Court allowed LPL to submit a maximum of five terms or phrases and CPT a maximum of eight. (D.I. 155.) Following the parties' submissions of the terms and phrases to be construed, LPL filed a Notice Of Voluntary Withdrawal Of Claims Relating To U.S. Patent No. 6,738,121 (D.I. 180). As a result of that withdrawal and the fact that one claim term was submitted by both parties, there are currently six claim terms and phrases in dispute: "interconnecting," "outer electrostatic discharge guard ring," "resistance," "corner pad," "removing said outer guard ring and row and column interconnections," and "pickup pad."

DISCUSSION

I. Legal Principles Of Claim Construction

Claim construction is a question of law. Markman v. Westview Instruments, Inc., 52 F.3d 967, 977-78 (Fed. Cir. 1995), aff'd, 517 U.S. 370, 388-90 (1996). In interpreting a claim, a court should look first to the intrinsic evidence, i.e. the patent itself, including the claims and the rest of the specification, and, if in evidence, the prosecution history. Vitronics Corp. v. Conceptor, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996). Although it is within the sound discretion of a court to use extrinsic evidence as an aid in construing a claim, extrinsic evidence is "unlikely to result in a reliable interpretation of patent claim scope unless considered in the

context of the intrinsic evidence." Phillips v. AWH Corp., 415 F.3d 1303, 1319 (Fed. Cir. 2005) (en banc).

A claim term should be construed to mean "what one of ordinary skill in the art at the time of the invention would have understood the term to mean." Markman, 52 F.3d at 986. However, "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." Phillips, 415 F.3d at 1313. Thus, the specification is usually "dispositive; it is the single best guide to the meaning of a disputed term." Id. at 1315 (quoting Vitronics, 90 F.3d at 1582). In other words, a claim term can be given its correct construction only within the context of "what the inventors actually invented and intended to envelop with the claim." Phillips, 415 F.3d at 1316.

II. Construction Of The Disputed Terms and Phrases

The language of independent claim 1 and dependent claims 3 and 7 is representative of the disputed terms and phrases. In full, claim 1 provides (emphasis added):

1. A method of manufacturing active matrix display backplanes and displays therefrom, comprising:
 - providing a substrate;
 - forming a pattern of pixels on said substrate;
 - forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;
 - forming an outer electrostatic discharge guard

ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and removing said outer guard ring and row and column interconnections prior to completion of the display.

('002 patent, col. 8, l. 65 - col. 9, l. 12.) In full, claim 3 provides (emphasis added): "3. The method as defined in claim 1 including forming at least one pickup pad coupled to said resistance via a shunt switching element." (Id. col. 9, ll. 16-18.) In full, claim 7 provides (emphasis added): "7. The method as defined in claim 1 including forming a corner pad on at least one corner of the display and aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections." (Id. col. 9, ll. 29-33.)

A. Construction of "Interconnecting"

LPL contends that the term "interconnecting" should be construed as "shorting." (D.I. 135 at 12.) LPL argues that "'interconnecting' was used throughout the entire intrinsic record in a manner consistent with this single meaning." (Id.) CPT contends that "shorting" is impermissibly vague because the specification uses that term in a variety of contexts. (D.I. 144 at 6.) CPT proposes instead the construction "electrically connecting with conductors." (D.I. 164 at 1.)

The Court agrees with CPT that LPL's proposed construction

is vague. Substituting "shorting" for "interconnecting" would not clarify the meaning of "interconnecting," but rather would make it more ambiguous. In the '002 patent's specification, "short" is used in at least four different ways: the path taken by an unintended, destructive discharge of a static potential ('002 patent, col. 2, ll. 57-62); a physical defect in electrical components resulting in an unintended current pathway (Id., col. 4, ll. 27-28); a deliberate re-routing of an electrostatic discharge via a shunt transistor (Id., col. 7, ll. 35-41); and a deliberate connection between electrical elements to provide an alternate current pathway (Id., col. 5, ll. 65-68). Only the last of these is consistent with LPL's proposed construction of "interconnecting".

LPL contends that CPT's proposed construction of "electrically connecting with conductors" improperly limits the term "interconnecting" to a single embodiment by specifying that the electrical connection must be made with conductors. (D.I. 158 at 2.) However, the consistent use of a claim term by the inventor in the specification may serve to limit the scope of a claim. Nystrom v. Trex Co., Inc., 424 F.3d 1136, 1145 (Fed. Cir. 2005). Here, CPT's proposed construction is consistent with the inventor's use of "interconnecting" throughout the '002 patent's

specification.¹ "Interconnecting" is consistently described or illustrated in figures as using "lines", "shorts", or "jumpers", i.e. conductors, to connect electrical elements. (See e.g., '002 patent, col. 5, ll. 65-68; col. 6, ll. 6-9; col. 6, ll. 42-43; col. 8, ll. 5-7.) Therefore, the Court will construe "interconnecting" to mean "electrically connecting with conductors."

B. Construction of "Removing Said Outer Guard Ring and Row and Column interconnections"

LPL contends that the phrase "removing said outer guard ring and row and column interconnections" does not require construction, but that the proper construction, if one is necessary, is "physically disconnecting said guard ring and row and column interconnections." (D.I. 135 at 23-24.) CPT's proposed construction is "electrically disconnecting the interconnections between rows and between columns, and electrically disconnecting rows and columns from the outer guard ring." (D.I. 137 at 12.) The Court agrees with LPL's construction.

The parties' dispute hinges on the meaning of "removing," with LPL contending that it means "physically disconnecting" and

¹ Defendants' proposed construction is also consistent with the use of "interconnecting" in U.S. Patent 4,820,222 ("the '222 patent"), which has the same inventor as the '002 patent and is incorporated by reference in the '002 patent. ('002 patent, col. 2, ll. 30-36.)

Defendants contending that it means "electrically disconnecting." CPT's construction depends on its assertion that "removing" means "removing a part or component from an electronic circuit." (D.I. 144 at 3; D.I. 138 at 9.) However, as it is used throughout the specification, "removing" is more logically interpreted as referring to the removal of the guard ring and row and column interconnections from the display panel. (See '002 patent, Abstract ("the external guard ring is removed prior to completion of the display"); col. 2, ll. 64-65 ("the external guard ring is removed at the end of the display manufacturing process"); col. 8, ll. 27-30 ("[t]he outer ESD guard ring . . . is removed prior to completion of the display").) Thus, the intrinsic evidence indicates that "removing" is used to mean physical disconnection and separation such that the outer guard ring and row and column interconnections are not included in the finished display panel. Therefore, the Court will construe "removing said outer guard ring and row and column interconnections" as "physically disconnecting said guard ring and row and column interconnections."

C. Construction of "Outer Electrostatic Discharge Guard Ring"

LPL's proposed construction of the phrase "outer electrostatic discharge guard ring" is "a closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges." (D.I. 158 at

2.) CPT's proposed construction is "a ring of conductor, located external to the inner electrostatic discharge guard ring if the two rings are used together, for draining off electrostatic buildup to prevent electrostatic discharge." CPT does not dispute that the outer guard ring is "a closed or open ring, or open L or C-shaped line." (D.I. 144 at 6.) The parties do dispute whether the guard ring functions to prevent electrostatic discharge ("ESD") or only to protect against damage caused by ESD.² The parties also dispute the meaning of "outer."

The specification consistently refers to the function of the ESD guard rings as protecting the active elements of the display from ESD rather than preventing ESD altogether. (See '002 patent, Abstract ("At least one ESD guard ring is provided to protect the active elements of the display from the potential discharge between the row and column lines."); col. 2, ll. 61-61 ("An external guard ring can be formed, which provides protection during manufacture of the displays . . ."); col. 8, ll. 27-29 ("The outer ESD guard ring provides ESD protection only during manufacture of the display . . .").) CPT points out that the specification uses the word "prevent" or "preventive" to describe the function of the ESD rings. (D.I. 164 at 4.) However, in

² CPT refers to this dispute as "insignificant," but, nevertheless, maintains the position that the proper construction refers to prevention of ESD rather than protection from ESD. (D.I. 164 at 4.)

both of the locations cited, the specification is referring to the prevention of damage caused by ESD rather than to the prevention of ESD itself.

The central dispute over the phrase "outer electrostatic discharge guard ring" is whether "outer" is used in reference to an inner ESD ring or to the entire display panel. CPT contends that "outer" must refer to the outer guard ring's position relative to the inner guard ring. (D.I. 137 at 8.) This contention is untenable. Independent claims 1 and 19 include an outer ESD guard ring, but no inner ESD guard ring. In the context of those claims, CPT's proposed construction would render the adjective "outer" meaningless.

On the other hand, LPL contends that "outer" refers to the outer guard ring's position relative to the active matrix display. CPT concedes that "active matrix display" as used in the '002 patent and in LPL's proposed construction means the entire finished display panel. (D.I. 164 at 3.) CPT argues that the Court should reject LPL's proposed construction because it is based on "the erroneous notion that the outer ring must be physically removed at the end of the manufacture." (Id.) As the Court concluded in section II.B. above, however, the intrinsic evidence indicates that physical removal of the outer guard ring is precisely what the patent teaches. Therefore, the Court will construe "outer electrostatic discharge guard ring" as "a closed

or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges."

D. Construction of "Resistance"

The parties agree that one of ordinary skill in the art would understand "resistance" to mean a physical property of a material or device characterized by opposition to the flow of electric current. (D.I. 135 at 13; D.I. 137 at 9.) They also agree that in the '002 patent, "resistance" is used to denote a circuit component. (D.I. 135 at 13; D.I. 160 at 2.) LPL contends that because "[a]ll circuit components . . . have the characteristic of resistance," the Court should construe "resistance" as "any component used to cause a voltage drop during current flow." (D.I. 135 at 13.) CPT's proposed construction is "[a] resistance, as it is used in the claims, means a resistor, which is a circuit element that has a specified resistance to the flow of electrical current. A resistance does not include switching elements such as transistors and diodes." (D.I. 137 at 9.)

LPL's proposed construction cannot be correct because, as CPT points out, (D.I. 137 at 12), it would exclude the single preferred embodiment that incorporates a "resistance." (See '002 patent, col. 8, ll. 1-48.) The only purposes stated for the "resistance" in that embodiment are to provide an "ESD short for

high electrostatic potentials . . . ,” (Id., col. 8, l. 31), and to minimize “the discharge current surge . . . ,” (Id., col. 8, l. 35). Thus, “resistance” as used in that embodiment, would not fall within the scope of LPL’s proposed construction of “any component used to cause a voltage drop during current flow.” A claim construction that excludes a preferred embodiment “is rarely, if ever, correct and would require highly persuasive evidentiary support. . . .” Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1583 (Fed. Cir. 1996) (citations omitted). The Court finds no such evidentiary support in this case.

On the other hand, CPT’s proposed construction unnecessarily limits “resistance” to one specific electric component, a resistor. There is no support in the intrinsic record for such a narrow interpretation. Moreover, a person skilled in the art would certainly understand the meaning of “resistor” so it is logical to conclude that the inventor would have chosen that term had he intended to refer only to that specific component.

LPL correctly notes, (D.I. 163 at 3), that it is improper to import limitations from a preferred embodiment into the claims. See JVW Enterprises, Inc. v. Interact Accessories, Inc., 424 F.3d 1324, 1335 (Fed. Cir. 2005). However, “there is sometimes a fine line between reading a claim in light of the specification, and reading a limitation into the claim from the specification.” Phillips v. AWH Corp., 415 F.3d 1303, 1323 (Fed.

Cir. 2005) (quoting Comark Communications, Inc. v. Harris Corp., 156 F.3d 1182, 1186-87 (Fed. Cir. 1998)). Here, because "resistance" is used in the claims in a manner somewhat different from its ordinary meaning to one of skill in the art, the only guidance as to how the Court should construe the term is how it is used in the single embodiment in which it appears. That embodiment mentions a "resistance" three times:

The [ESD guard ring] line 210 is connected to the other set of gate or source lines by a shunt line 224, a shunt transistor 226 and a large resistance 228, such as 100 K ohms (illustrated schematically). . . . The resistance provides an ESD short for high electrostatic potentials which can be incurred during manufacturing The resistance minimizes the discharge current surge

('002 patent, col. 8, ll. 23-34.) In the claims, the term "resistance" is used consistently to denote only a circuit component used to couple the outer ESD guard ring to the interconnected row and column lines and the pickup pad. (See e.g. Id., col. 9, ll. 63-65; col. 10, ll. 6-8.)

Reading the claims in light of the specification, which describes the "resistance" only in general terms, the Court concludes that the patentee intended the claims and this embodiment in the specification to be coextensive at least in regard to the term "resistance".³ Therefore, the Court will

³ The Court also notes that the patentee explicitly stated that certain elements of the invention could vary from the specific descriptions in that embodiment, but did not include the "resistance" among those elements. ('002 patent, col. 8, ll. 49-

construe "resistance" as "a circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from an electrostatic discharge."

E. Construction of "Corner Pad"

LPL contends that the term "corner pad" does not require construction, but that the proper construction, if one is necessary is "a reference mark for cutting" (D.I. 135 at 24.) CPT contends that the Court should construe "corner pad" as "a pad of metal or other conductive materials that is located at the corner of an outer guard ring, and electrically connected with the outer ring" (D.I. 137 at 15.) CPT argues, (Id.), and LPL does not dispute, that "corner pad" has no inherent meaning to one of ordinary skill in the art and thus can be understood only within the context of the '002 patent's claims and specification. LPL does concede that "[o]ne of ordinary skill in the art would understand the term 'pad' to be a conductive area." (D.I. 135 at 15; D.I. 143 at 15.)

The term "corner pad" appears in only one embodiment in the specification. (See '002 patent, col. 8, ll. 1-48.) That embodiment describes three features of a "corner pad." First, it is connected to each other corner pad by conductive lines of the outer guard ring. (Id., col. 8, ll. 8-11.) Second, it can be grounded. (Id., col. 8, ll. 11-12.) Third, it provides

alignment for the scribe lines. (Id., col. 8, ll. 12-15.) The second feature is explicitly optional, so it need not be included in the Court's construction. The third feature is specifically claimed, so it too need not be included in the Court's construction. (See, e.g., Id., col. 9, ll. 29-33 ("7. The method as defined in claim 1 including forming a corner pad on at least one corner of the display and aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections.")) Therefore, the Court concludes that LPL's proposed construction of "a reference mark for cutting" is unnecessary and would be redundant. The location of the corner pad is also specifically claimed as being "on at least one corner of the display." (See, e.g., Id., col. 9, l. 30.) Thus CPT's inclusion of "located at the corner of an outer guard ring" in its proposed construction is both unnecessary and inaccurate.

The remaining issue is whether the "corner pad" must be electrically connected to the outer guard ring. CPT bases its contention that the "corner pad" must be "electrically connected with the outer ring" on a single sentence from the specification: "A corner pad 208 is connected to each other corner pad (not illustrated) by respective outer conductive lines 210 and 212 of the guard ring 200." (Id., col. 8, ll. 8-11.) The Court concludes that it would be improper to import this limitation from the specification into the claims. Therefore, to the extent

that "corner pad" requires construction, the Court will construe it as "an area of conductive material."

F. Construction of "Pickup Pad"

LPL's proposed construction of "pickup pad" is "a conductive area used to electrically connect the back plane to the front plane" (D.I. 135 at 14.) CPT's proposed construction is "a pad located at the corner region of a backplane for aligning the frontplane and backplane" (D.I. 137 at 13.) CPT contends, and LPL does not dispute, that the term "pickup pad" has no inherent meaning to one of ordinary skill in the art, and thus, can be understood only within the context of the intrinsic evidence. (D.I. 137 at 13.) The parties agree, however, that "pad" would be understood by one of ordinary skill in the art to mean a conductive area. (D.I. 135 at 15; D.I. 143 at 15; D.I. 160 at 3.) The Court concludes that neither proposed construction is appropriate and will decline to construe "pickup pad."

LPL's contention that the "pickup pad" is used to electrically connect the back plane to the front plane has no support in the intrinsic evidence. Neither the specification nor the claims of the '002 patent mentions any electrical connection between the front plane and the back plane via the "pickup pad". Both teach only the electrical connection of the "pickup pad" with other elements on the back plane. Thus, LPL's proposed construction cannot be correct.

CPT's proposed construction would violate the doctrine of claim differentiation. In this context, claim differentiation "refers to the presumption that an independent claim should not be construed as requiring a limitation added by a dependent claim." Curtiss-Wright Control Corp. v. Velan, Inc., 438 F.3d 1374, 1380 (Fed. Cir. 2006) (citing Nazomi Communications, Inc. v. Arm Holdings, PLC., 403 F.3d 1364, 1370 (Fed. Cir. 2005)). In the '002 patent, claim 5 depends from claim 3.⁴ Claim 3 claims "[t]he method as defined in claim 2 including forming at least one pickup pad coupled to said resistance via a shunt switching element." ('002 patent, col. 9, ll. 16-18.) Claim 5 claims "[t]he method as defined in claim 3 including forming a corner on the said pad to align the front plane and back plane of the display." (Id., col. 9, ll. 23-25.) To construe "pickup pad" as CPT proposes, as "a pad . . . for aligning the frontplane and backplane," would be to read the limitation from claim 5 into claim 3, rendering claim 5 superfluous and violating the doctrine of claim differentiation.

All of the significant attributes of the "pickup pad" mentioned in the specification are also specifically claimed. (Compare, '002 patent, col. 8, ll. 18-39, with id. col. 9, ll. 16-28.) Therefore, the Court concludes that no further

⁴ The discussion that follows applies identically to claims 16 and 14, 23 and 21, and 34 and 32.

construction of the term "pickup pad" is necessary.

CONCLUSION

An Order consistent with this Memorandum Opinion will be entered setting forth the meaning of the disputed terms and phrases in the '002 patent.

EXHIBIT 4

**ANSI/IEEE Std 100-1988
Fourth Edition**

**IEEE
Standard Dictionary
of
Electrical and
Electronics
Terms**

**Frank Jay
Editor in Chief**

**J. A. Goetz
Chairman
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on Definitions (SCC 10)**

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Buckley, F. J.	Kieburz, R. B.	Smith, E. P.
Cannon, J. B.	Kincaid, M. R.	Smolin, M.
Cantrell, R. W.	Klein, R. J.	Snyder, J. H.
Chartier, V. L.	Klopfenstein, A.	Spurgin, A. J.
Cherney, E. A.	Koepfinger, J. L.	Stephenson, D.
Compton, O. R.	Lensner, W.	Stepniak, F.
Costrell, L.	Masiello, R. D.	Stewart, R. G.
Davis, A. M.	Meitzler, A. H.	Swinth, K. L.
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Donnan, R. A.	Migliaro, H. W.	Thomas, L. W., Sr.
Duvall, L. M.	Mikulecky, H. W.	Vance, E. E.
Elliott, C. J.	Moore, H. R.	Wagner, C. L.
Erickson, C. J.	Mukhedar, D.	Walter, F. J.
Flick, C.	Muller, C. R.	Weinschel, B. O.
Freeman, M.	O'Donnell, R. M.	Zitovsky, S. A.
	Petersons, O.	



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November 3, 1988

SH12070

residual induction

828

resistance bridge smoke detector

resistance-

residual induction (1) (magnetic material). The magnetic induction corresponding to zero magnetizing force in a material that is in a symmetrically cyclically magnetized condition. 210

(2) (residual flux density) (toroidal magnetic amplifier cores). The magnetic induction at which the magnetizing force is zero when the magnetic core is cyclically magnetized with a half-wave sinusoidal magnetizing force of a specified peak magnitude. *Note:* This use of the term residual induction differs from the standard definition that requires symmetrically cyclically magnetized conditions. 165

residual magnetism (ferromagnetic bodies). A property by which they retain a certain magnetization (induction) after the magnetizing force has been removed. 244, 210

residual modulation. *See:* carrier noise; carrier noise level.

residual probe pickup (constancy of probe coupling) (slotted line). The noncyclical variation of the amplitude of the probe output over its complete range of travel when reflected waves are eliminated on the slotted section by proper matching at the output and the input, discounting attenuation along the slotted section. It is defined by the ratio of one-half of the total variation to the average value of the probe output, assuming linear amplitude response of the probe, at a specified frequency(ies) within the range of usage. *Note:* This quantity consists of two parts of which one is reproducible and the other is not. The repeatable part can be eliminated by subtraction in repeated measurements, while the nonrepeatable part must cause an error. The residual probe pickup depends to some extent on the insertion depth of the probe. *See:* measurement system; residual standing-wave ratio. 185

residual reflected coefficient (reflectometer). The erroneous reflection coefficient indicated when the reflectometer is terminated in reflectionless terminations. *See:* measurement system. 185

residual relay (power switchgear). A relay that is so applied that its input, derived from external connections of instrument transformers, is proportional to the zero-phase-sequence component of a polyphase quantity. 103

residual response (1) (non-real time spectrum analyzer). A spurious response in the absence of an input. 68

(2) (spectrum analyzer). A spurious response in the absence of an input, not including noise and zero pickup. 390

residual standing-wave ratio (SWR) (slotted line). The standing-wave ratio measured when the slotted line is terminated by a reflectionless termination and fed by a signal source that provides a nonreflecting termination for waves reflected toward the generator. *Note:* Residual standing-wave ratio does not include the residual noncyclical probe pickup or the attenuation encountered as the probe is moved along the line. *See:* residual probe pickup. 185

residual voltage (1) (arrestor) (discharge voltage). The

voltage that appears between the line and ground terminals of an arrestor during the passage of discharge current. *See:* inductive coordination. 308, 62

(2) (protective relaying). The sum of the three line-to-neutral voltages on a three-phase circuit. 128

residue check (computing systems). A check in which each operand is accompanied by the remainder obtained by dividing this number by n , the remainder then being used as a check digit or digits. *See:* modulo n check. 255, 77

resin (rotating machinery). Any of various hard brittle solid-to-soft semisolid amorphous fusible flammable substances of either natural or synthetic origin: generally of high molecular weight, may be either thermoplastic or thermosetting. 63

resin-bonded paper-insulated bushing (outdoor electric apparatus). A bushing in which the major insulation is provided by paper bonded with resin. 168

resist (electroplating). Any material applied to part of a cathode or plating rack to render the surface nonconducting. *See:* electroplating. 328

resistance (1) (network analysis). (A) That physical property of an element, device, branch, network, or system that is the factor by which the mean-square conduction current must be multiplied to give the corresponding power lost by dissipation as heat or as other permanent radiation or loss of electromagnetic energy from the circuit. (B) The real part of impedance. *Note:* Definitions (A) and (B) are not equivalent but are supplementary. In any case where confusion may arise, specify definition being used. *See:* resistor. 210, 185, 206

(2) (shunt). The quotient of the voltage developed across the instrument terminals to the current passing between the current terminals. In determining the value, account should be taken of the resistance of the instrument and the measuring cable. The resistance value is generally derived from a direct-current measurement such as by means of a double Kelvin bridge. *See:* test voltage and current. 307

(3) (automatic control). A property opposing movement of material, or flow of energy, and involving loss of potential (voltage, temperature, pressure, level). 56

(4) (antenna). *See:* antenna resistance; radiation resistance.

resistance, apparent (insulation testing). Ratio of the voltage across the electrodes in contact with the specimen to the current between them as measured under the specified test conditions and specified electrification time. 97

resistance box. A rheostat consisting of an assembly of resistors of definite values so arranged that the resistance of the circuit in which it is connected may be changed by known amounts. 210

resistance braking. A system of dynamic braking in which electric energy generated by the traction motors is dissipated by means of a resistor. *See:* dynamic braking. 328

resistance bridge smoke detector (fire protection devices). A device which responds to an increase of

smoke particles
combustion
these conditions
reduce the
tor to response
resistance-
between two
by means of
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resistance-
scopes). The
capacitance to
scope.
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with the resistan

EXHIBIT 5



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New York

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EXHIBIT 6



US005156986A

United States Patent [19]

Wei et al.

[11] **Patent Number:** 5,156,986[45] **Date of Patent:** Oct. 20, 1992

[54] **POSITIVE CONTROL OF THE SOURCE/DRAIN-GATE OVERLAP IN SELF-ALIGNED TFTS VIA A TOP HAT GATE ELECTRODE CONFIGURATION**

[75] **Inventors:** Ching-Yeu Wei; George E. Possin; Robert F. Kwasnick, all of Schenectady, N.Y.

[73] **Assignee:** General Electric Company, Schenectady, N.Y.

[21] **Appl. No.:** 667,149

[22] **Filed:** Mar. 11, 1991

Related U.S. Application Data

[62] Division of Ser. No. 593,423, Oct. 5, 1990, abandoned.

[51] **Int. Cl.⁵** H01L 21/336; H01L 21/28

[52] **U.S. Cl.** 437/40; 437/44; 437/101; 437/909; 357/23.7

[58] **Field of Search** 437/40, 41, 44, 101, 437/245, 246, 228, 909; 156/649, 656, 667; 357/4, 23.7, 2

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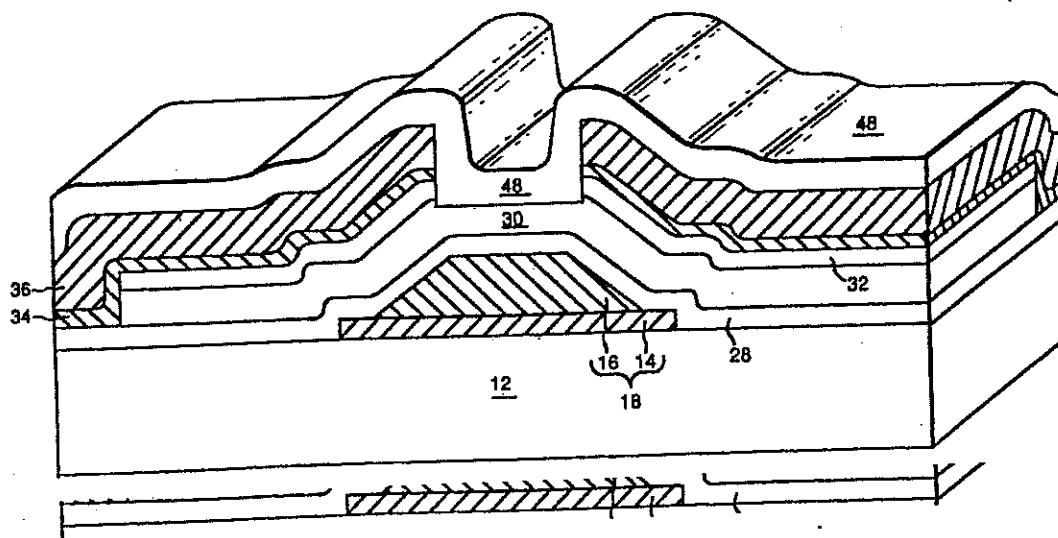
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Primary Examiner—Mary Wilczewski
Attorney, Agent, or Firm—Donald S. Ingraham; James C. Davis, Jr.; Marvin Snyder

ABSTRACT

[57] Positive control over the length of the overlap between the gate electrode and the source and drain electrodes in a thin film transistor is provided by a gate conductor layer comprising two different conductors having differing etching characteristics. As part of the gate conductor pattern definition process, both gate conductors are etched to expose the underlying material and the upper gate conductor layer is etched back to expose the first gate conductor layer in accordance with the desired overlap between the gate electrode and the source and drain electrodes. Thereafter, the remainder of the device is fabricated with the source and drain electrodes self-aligned with respect to the second gate conductor layer using a planarization and non-selective etch method.

13 Claims, 15 Drawing Sheets



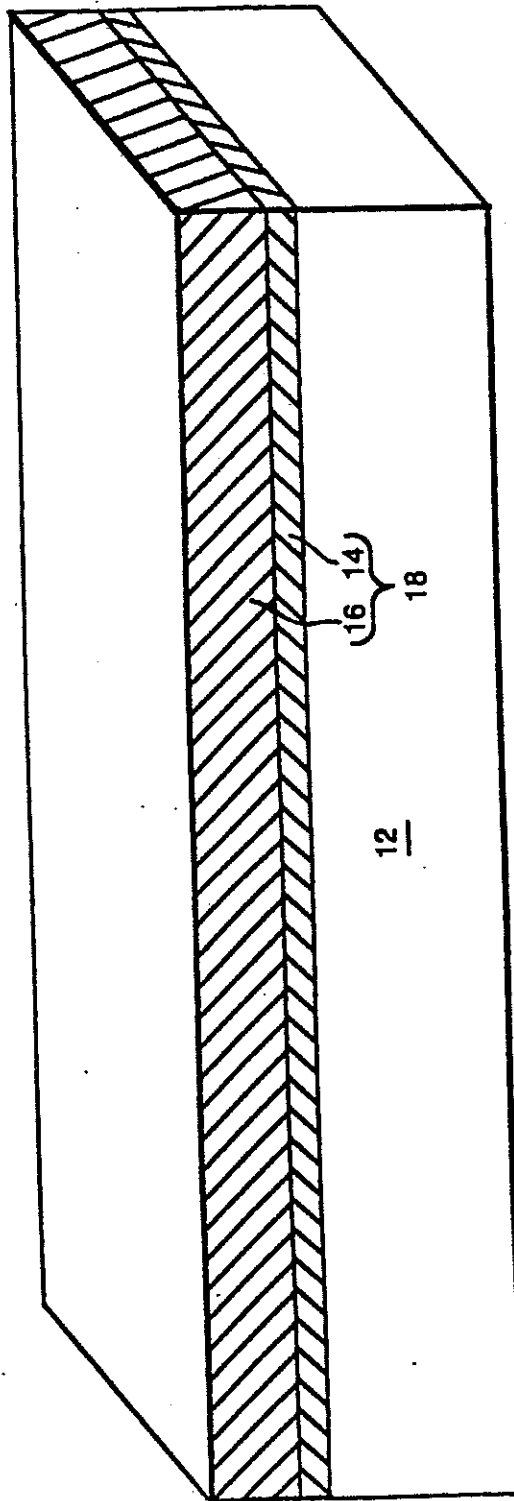
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FIG. 1



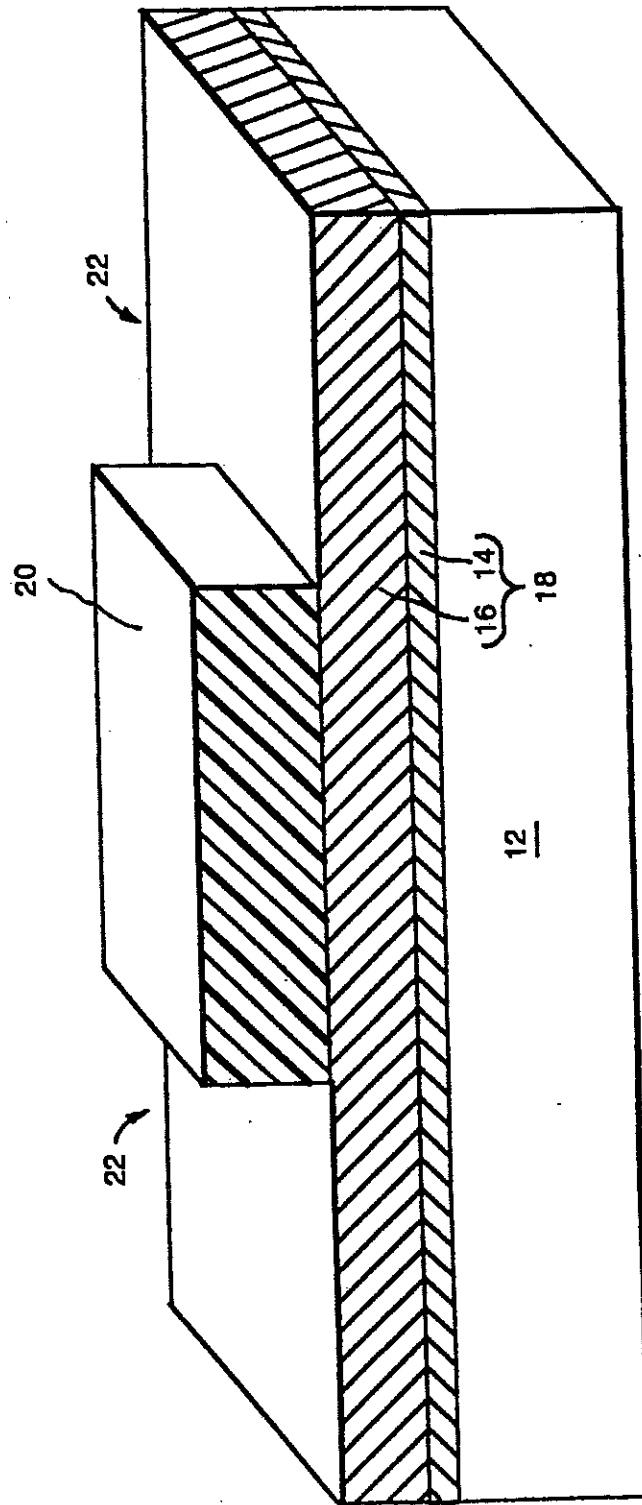
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FIG. 2



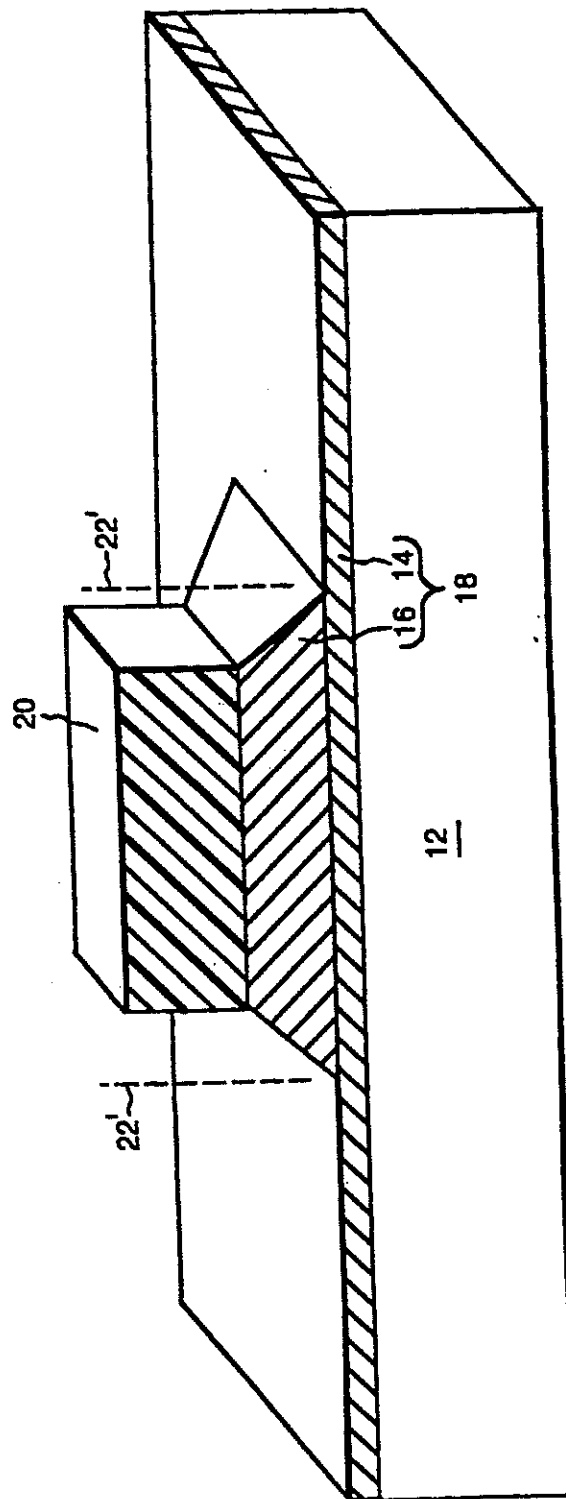
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FIG. 3



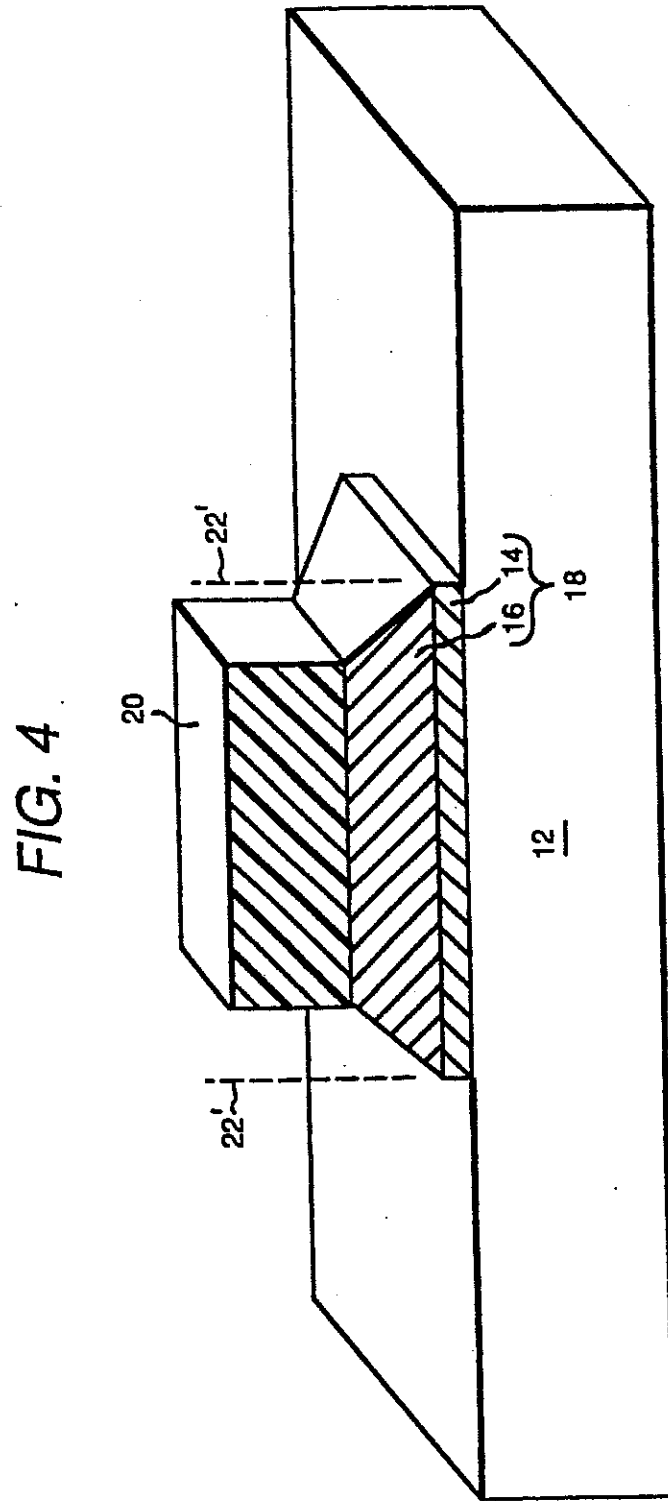
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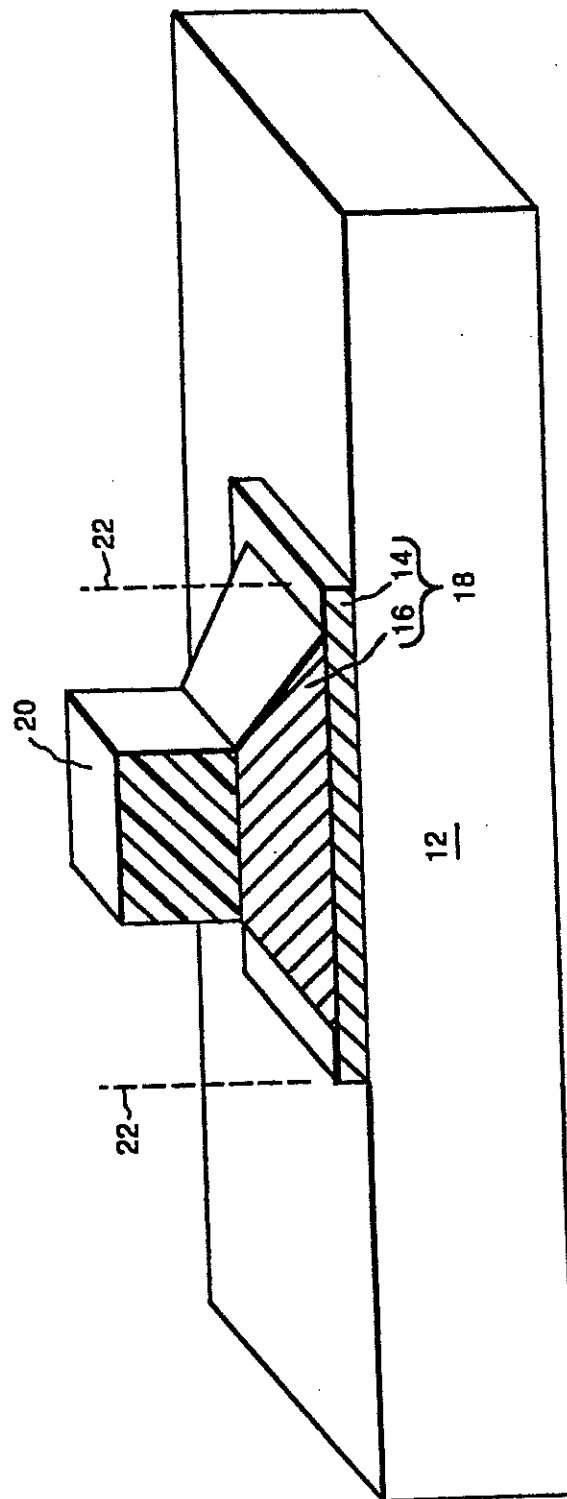
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FIG. 5



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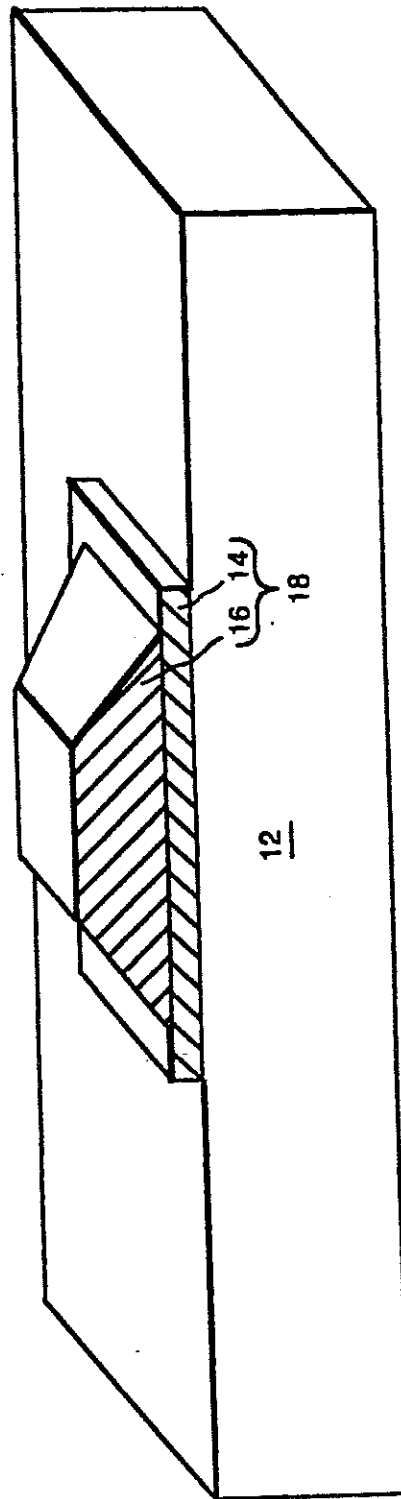
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FIG. 6



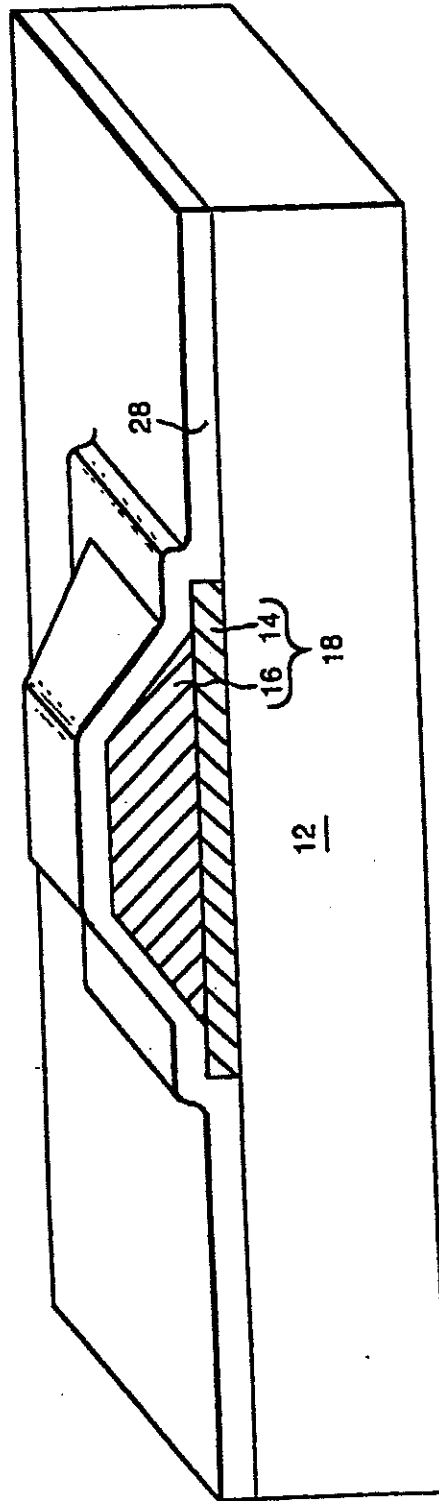
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FIG. 7



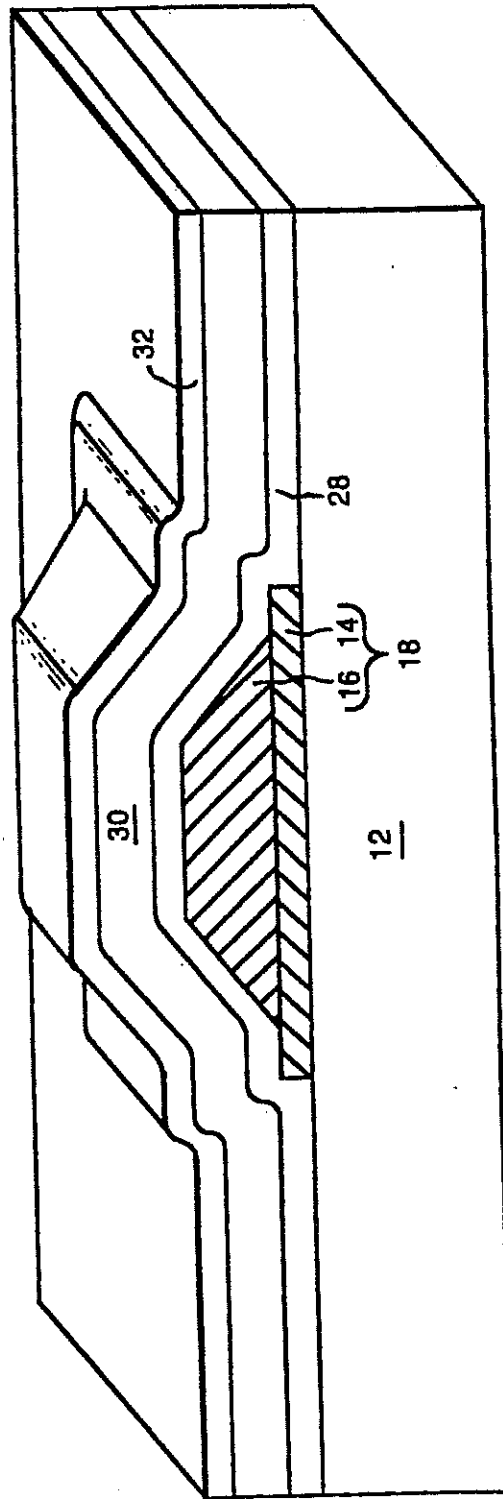
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FIG. 8



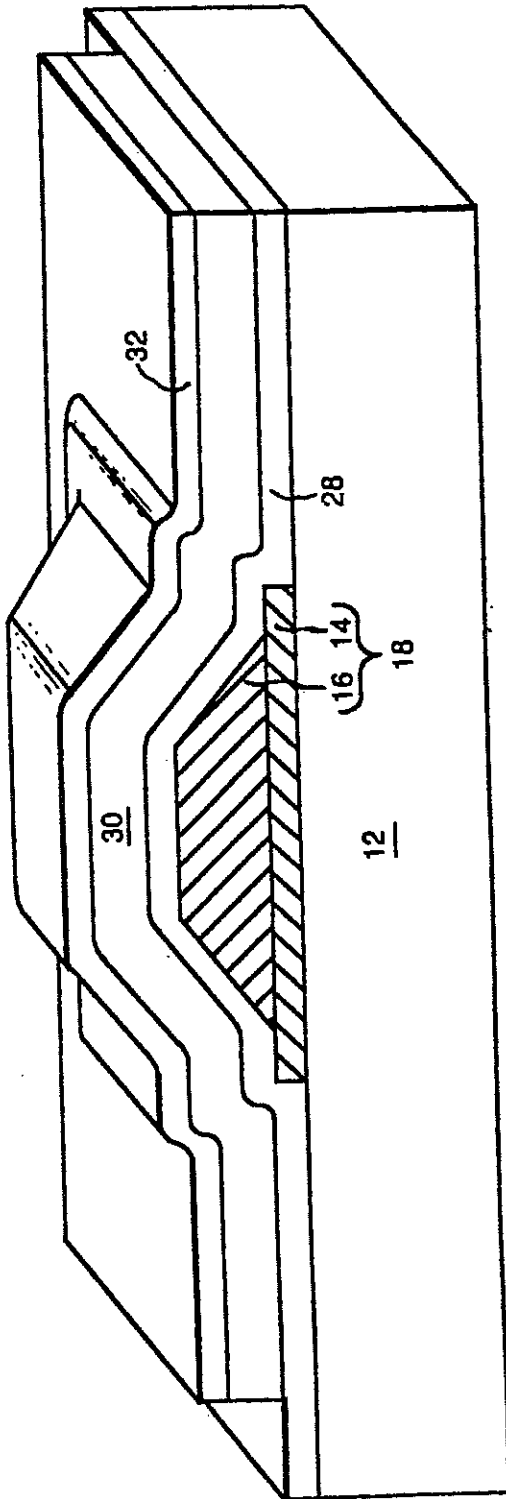
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FIG. 9



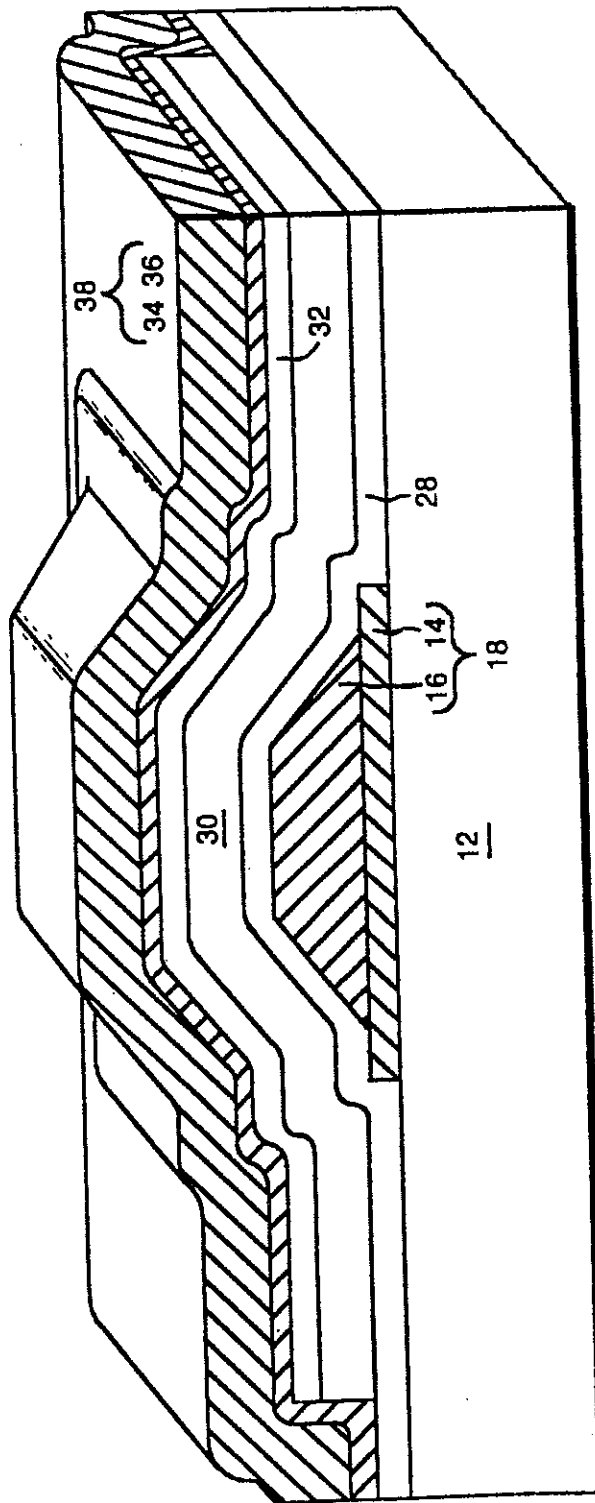
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FIG. 10



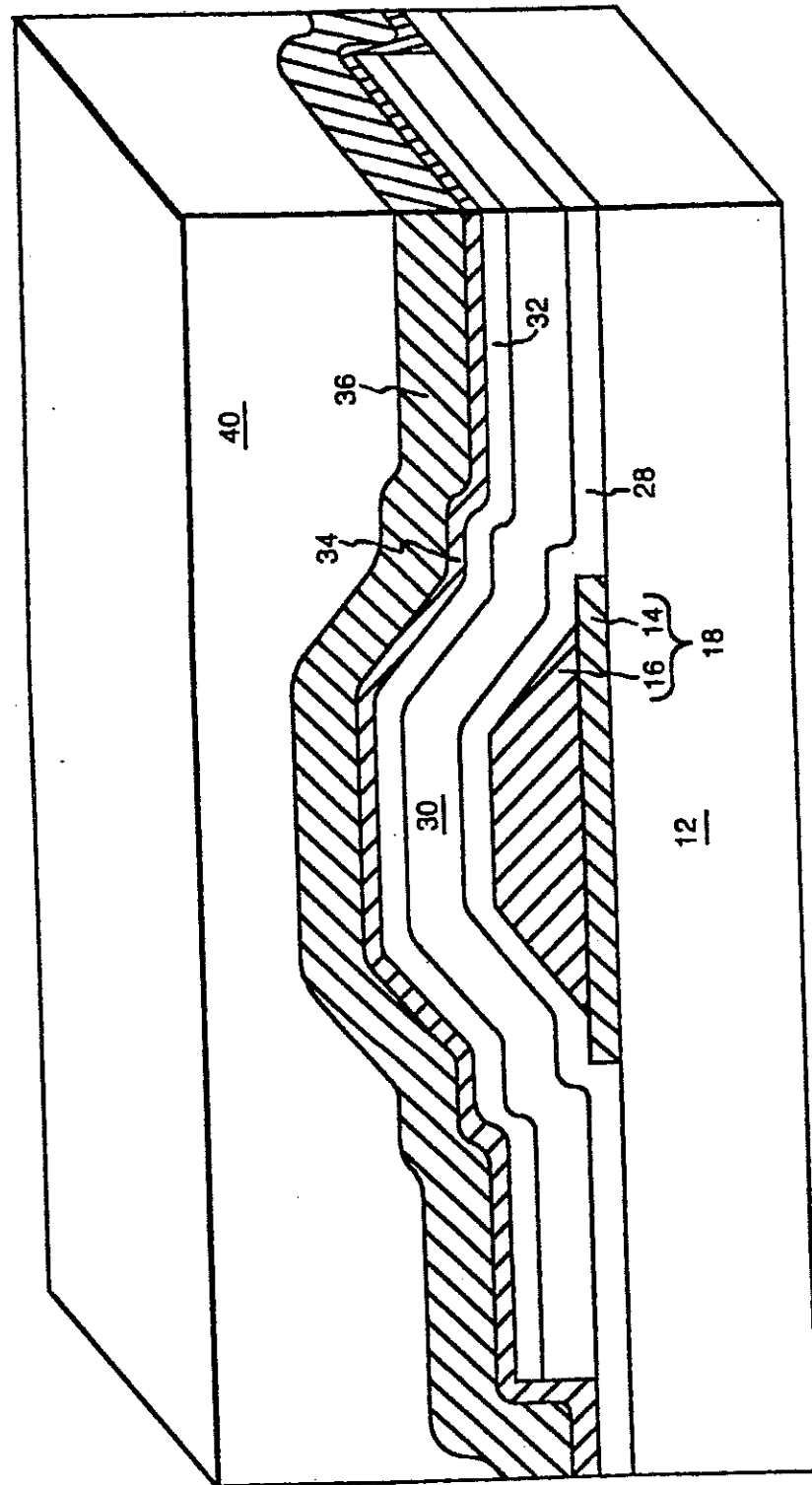
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FIG. 11



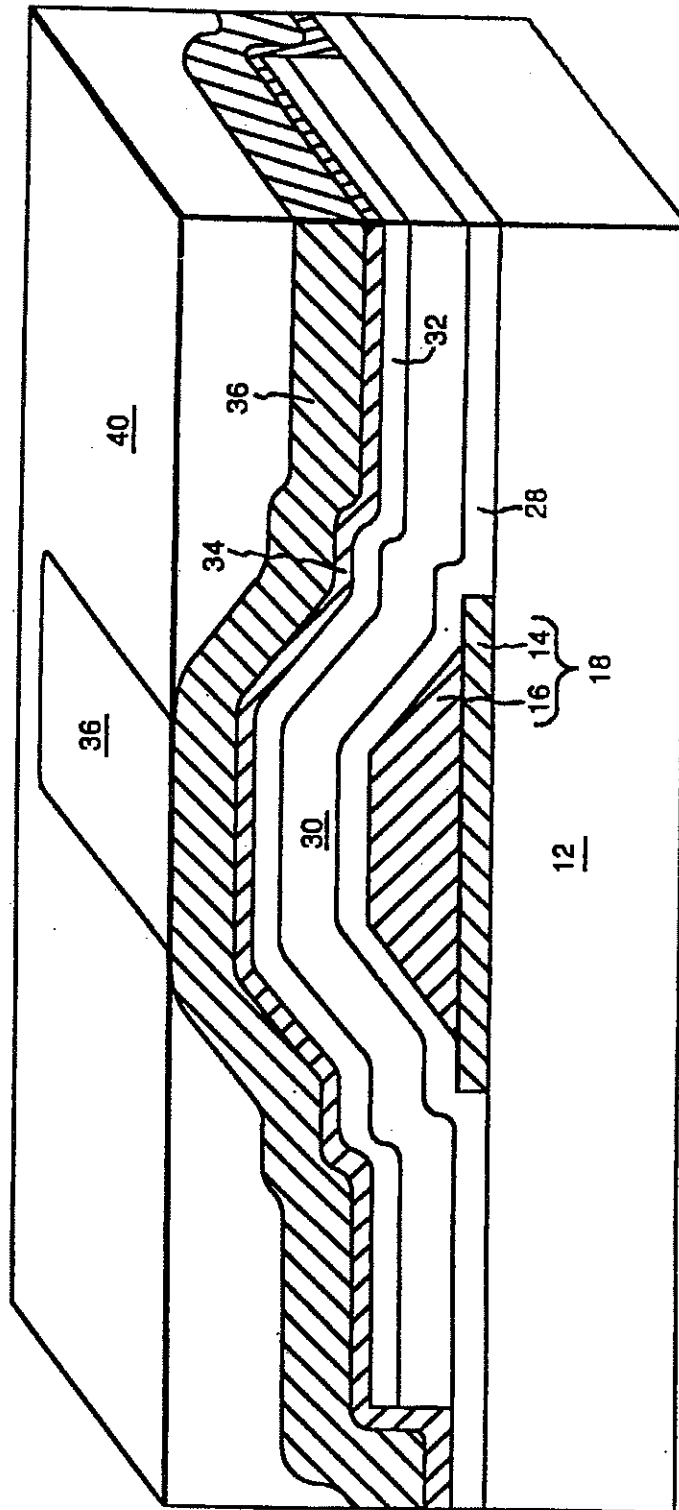
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FIG. 12



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FIG. 13

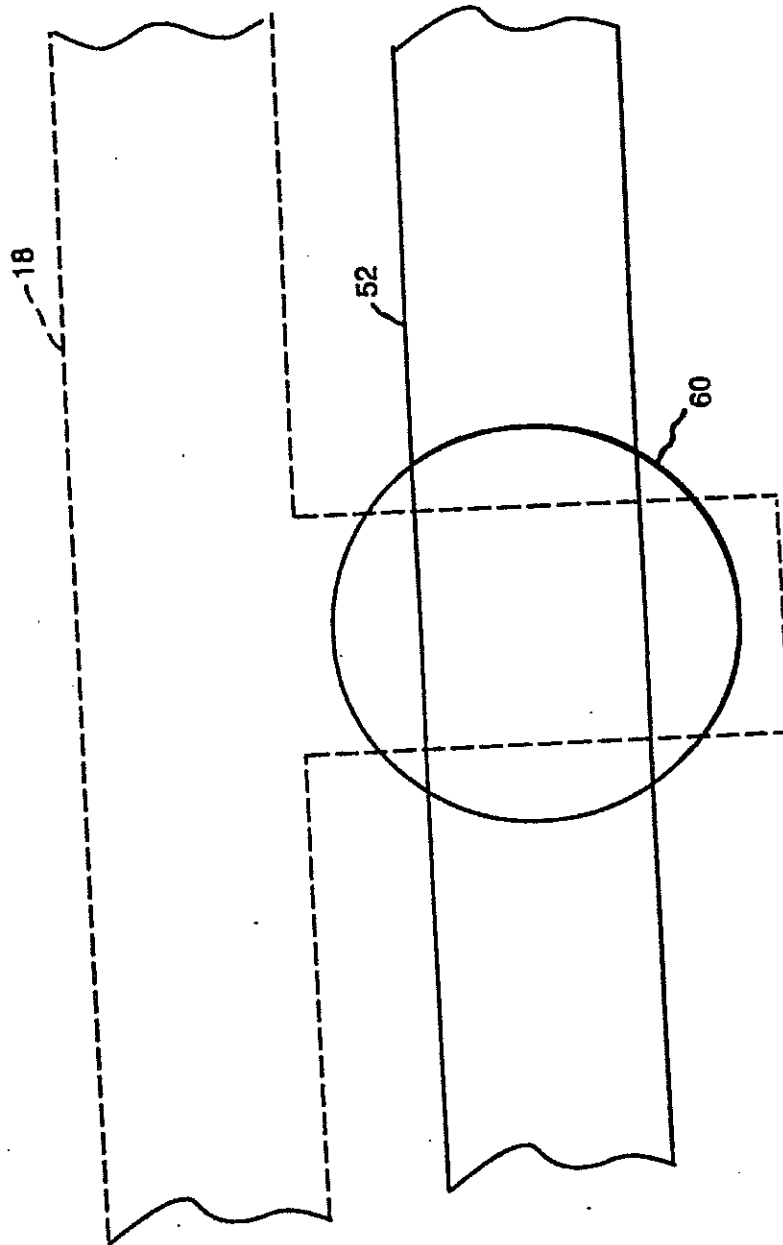
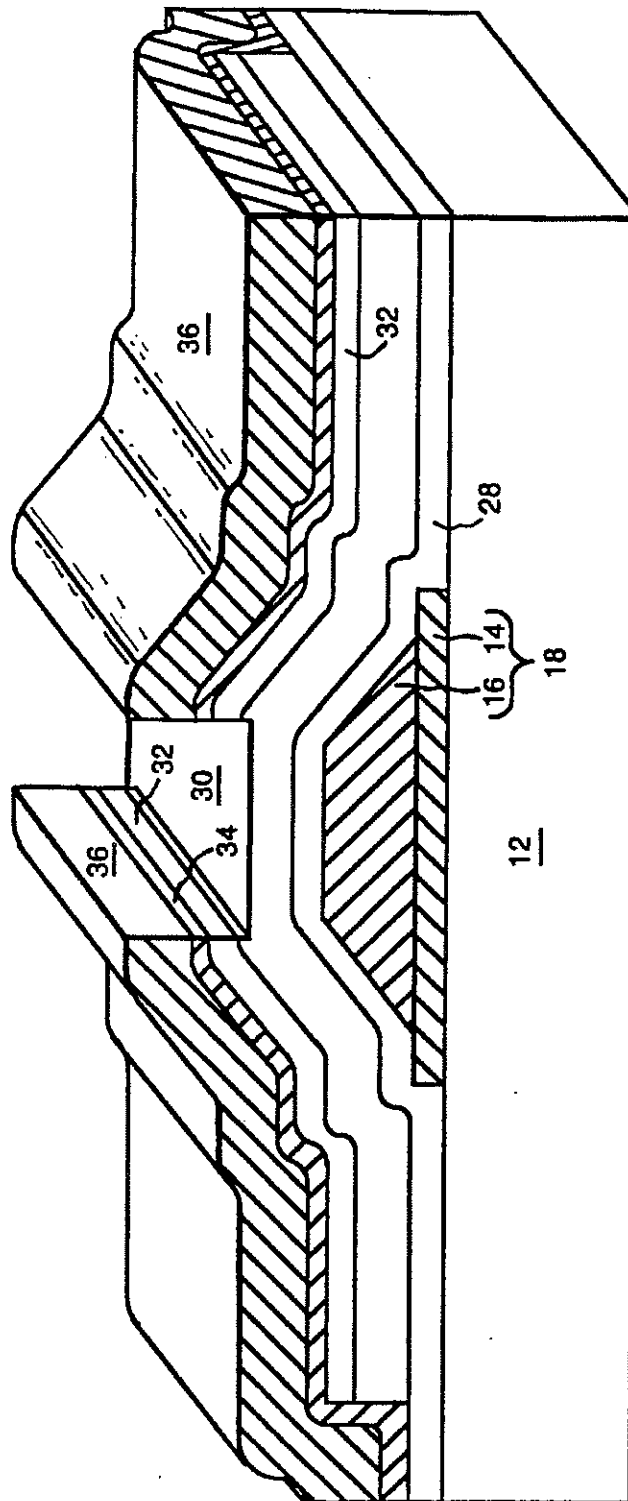


FIG. 14



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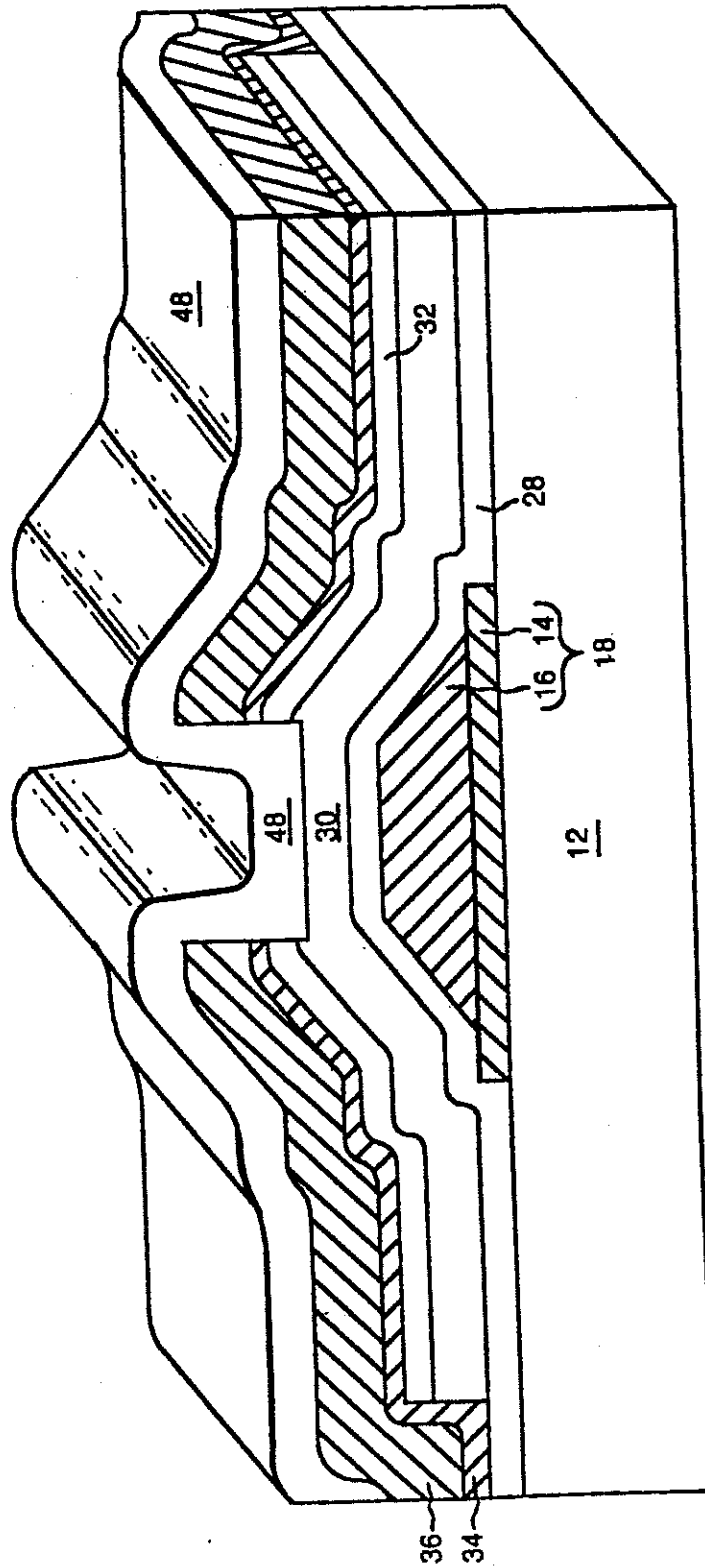
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FIG. 15



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1

POSITIVE CONTROL OF THE SOURCE/DRAIN-GATE OVERLAP IN SELF-ALIGNED TFTS VIA A TOP HAT GATE ELECTRODE CONFIGURATION

This application is a division of application Ser. No. 07/593,423, filed Oct. 5, 1990, now abandoned.

RELATED APPLICATIONS

The present application is related to application Ser. No. 07/593,419, filed Oct. 5, 1990, entitled, "Thin Film Transistor Structure With Improved Source/Drain Contacts", by R. F. Kwasnick, et al.; application Ser. No. 07/593,425, filed Oct. 5, 1990, entitled "Device Self-Alignment by Propagation of a Reference Structure's Topography", by C-Y Wei, et al.; application Ser. No. 07/593,421, filed Oct. 5, 1990, entitled, "Thin Film Transistor Having an Improved Gate Structure and Gate Coverage by the Gate Dielectric" by R. F. Kwasnick, et al.; application Ser. No. 07/510,767, filed Apr. 17, 1990, entitled "Method for Photolithographically Forming a Self-Aligned Mask Using Back Side Exposure and a Non-Specular Reflecting Layer", by G. E. Possin, et al.; and application Ser. No. 07/499,733, filed Mar. 21, 1990, entitled "Method for Fabricating a Self-Aligned Thin-Film Transistor Utilizing Planarization and Back-Side Photoresist Exposure", by G. E. Possin, et al., now U.S. Pat. No. 5,010,027, each of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to the field of fabrication techniques for thin film transistors, and more particularly to techniques for self-aligned fabrication of thin film transistors.

Background Information

Thin film transistors (TFTs) are employed in liquid crystal displays and imagers to control or sense the state of each pixel of the display or image. At present, such thin film transistors are typically fabricated from amorphous silicon. In such display or sensor systems, system operating characteristics are optimized by making each cell or pixel have substantially identical operating characteristics. These operating characteristics include switching speed, capacitive loading of drive and sense lines, the gain of transistors and so forth.

One of the processing problems which causes variation in the characteristics of different cells within such structures is the inability to accurately align the position of a mask which defines the source and drain electrodes of thin film transistors in a manner which ensures that the source/drain electrodes are accurately aligned with respect to the gate electrodes. Misalignment results in an increase in the overlap between the gate electrode and either the source electrode or the drain electrode with a corresponding decrease in the overlap between the gate and the other of them. Since the capacitances between the gate electrode and the source or drain electrodes are direct functions of the overlap between them, such a change in overlap produces a change in device's capacitances and consequently, switching speed and loading of other circuits. The possibility of misalignment requires that the size of the gate metal be increased to ensure that all devices have acceptable overlap between the gate and the source and drain. This

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increases the device size and hence the total capacitance per device. The device capacitance is important because it controls the charging time of the gate electrodes, the capacitive coupling between the gate and the source and drain nodes, and the noise introduced by the defects in the amorphous silicon or at the amorphous silicon/dielectric interface. Consequently, there is a desire to provide self-alignment between the source and drain electrodes and the gate electrode in order to maintain a fixed, predictable overlap between the gate electrode and each of the source and drain electrodes across an entire wafer.

A variety of self-alignment techniques have been proposed or developed. The above-identified related applications Ser. Nos. 07/499,733 and 07/510,767 each disclose techniques for obtaining self-alignment between the gate electrode and the source and drain electrodes through the use of through-the-substrate exposure of photoresist. Such processes result in specific gate-to-source and gate-to-drain overlaps which are peculiar to those techniques and the particular manner in which they are carried out. Those overlaps may be smaller or larger than optimum. Such a through-the-substrate exposure technique is not suitable where the semiconductor itself or another device layer would absorb the light needed to expose the photoresist. Consequently, there is a need for other self-alignment techniques for thin film transistors.

Related application Ser. No. 07/593,425 solves these problems by employing mechanical propagation of topographical features of a lower, reference layer, upward through subsequently deposited layers of the structure, including a support layer. A subordinate layer (source/drain metallization) is deposited on the support layer and may be either conformal or not conformal. If necessary, a planarization layer is formed over the subordinate layer to provide a planar upper surface for the structure. Material is then removed from the upper surface in a non-selective, uniform manner until the source/drain metallization becomes exposed in an aperture which is thereby created in the planarization layer in alignment with the underlying reference layer pattern. The exposed portion of the subordinate layer is then selectively etched to expose the support layer. Alternatively, the planarization etch could be continued until the support layer was exposed, but that would result in thinner source and drain electrodes. Other portions of the subordinate layer are then patterned, if necessary and the fabrication of the device completed. The result is a device in which the overlap of the subordinate layer over the reference pattern in the vicinity of the aperture in the subordinate layer is self-aligned with respect to the reference layer pattern.

The technique of application Ser. No. 07/593,425 can provide a very short overlap between the gate electrode and the source and drain electrodes. In particular, an overlap of less than 0.5 μm is achievable. Such a small overlap is desirable from the point of view of minimizing overlap capacitance and capacitance induced noise. Unfortunately, it is found experimentally that there is a minimum overlap between the gate and the source and drain electrodes below which the saturation drain current of a TFT degrades significantly. While the minimum length of this overlap for good device operating characteristics may vary with different semiconductor materials and other variations in the device structure, it would be desirable to have a technique for positively

5,156,986

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controlling the amount of overlap between the gate electrode and the source and drain electrodes in a self-aligned TFT structure.

OBJECTS OF THE INVENTION

Accordingly, a primary object of the present invention is to provide a technique for positively controlling the length of the overlap between the gate electrode and the source and drain electrodes in a self-aligned thin film transistor.

Another object of the present invention is to increase the versatility of the self-alignment technique disclosed in related application Ser. No. 07/593,425.

Another object of the present invention is to provide a self-alignment method which is applicable to opaque substrates.

SUMMARY OF THE INVENTION

The above and other objects which will become apparent from the specification as a whole, including the drawings, are accomplished in accordance with the present invention by fabricating the gate electrode as two separate layers of different conductors; patterning the entire gate electrode to the desired gate electrode pattern and subsequently etching the second layer of the gate electrode conductor back from the edges of the first level gate electrode conductor in a self-aligned manner whereby positive control of the degree of setback of the tapered edge of the upper layer (thick) gate conductor material from the lower layer (thin) conductor material is provided while retaining self-alignment. In this manner, a self-aligned process which relies on propagation of the topography of the gate electrode through subsequently deposited layers of the structure provides gate-to-source and gate-to-drain electrode overlaps which are controlled by the setback of the second gate conductor layer with respect to the first gate conductor layer in addition to the setback produced by the slope of the tapered second gate conductor layer.

In accordance with one embodiment of the invention, the first and second gate conductor layers are sequentially deposited on a substrate in the same vacuum pumpdown, the gate conductor is photomasked and etched to expose the substrate in the areas where the gate conductor is not desired. Thereafter, the second gate conductor layer is etched back from the edge of the first conductor layer using the same gate mask and an etchant to which the first gate conductor layer is substantially immune and with a technique which tapers the second gate conductor layer to provide lateral edges on that layer which are suitable for the deposition of conformal layers thereover. Thereafter, substantially conformal gate dielectric and semiconductor layers are deposited on the structure followed by patterning of the semiconductor layers and then deposition of source/-drain metallization which may be conformal or nonconformal. Where the source/drain metallization does not exhibit a planar upper surface, a planarization layer is deposited on top of the source/drain metallization to provide a planar upper surface for the device structure. The device structure is then etched in a non-selective manner until the source/drain metallization is exposed in alignment with the raised (thick) portion of the gate electrode pattern. The exposed portion of the source/-drain metallization is then selectively etched to expose the n^+ amorphous silicon which is then removed. Thereafter, back channel passivation may be provided

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on the upper surface of the structure to minimize the effect of external conditions on the operating characteristics of the device.

The resulting semiconductor device has a setback or top hat gate conductor configuration in which the effective electrical gate width is that of the thin, lower, wider gate conductor layer while the configuration of the thicker, upper, narrower gate conductor layer controls the self-alignment of the source and drain electrodes with respect to the gate electrode and thus the overlap between the source and drain electrodes and the gate electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of practice, together with further objects and advantages thereof, may best be understood by reference to the following description taken in connection with the accompanying drawings in which:

FIGS. 1-14 illustrate successive stages in the fabrication of a thin film transistor in accordance with the present invention;

FIG. 1 is a perspective, partially cross section view of a substrate having an unpatterned reference layer disposed thereon;

FIG. 2 is a perspective, partially cross section view of the FIG. 1 structure having a patterned layer of photoresist disposed thereon;

FIG. 3 is a perspective, partially cross section view of the FIG. 2 structure following etching of an upper gate conductor layer;

FIG. 4 is a perspective, partially cross section view of the FIG. 3 structure following etching of a lower gate conductor layer;

FIG. 5 is a perspective, partially cross section view of the structure following etch back of the upper layer of the gate conductor from the edge of the lower gate conductor;

FIG. 6 is a perspective, partially cross-section view of the FIG. 5 structure following stripping of the retained photoresist;

FIG. 7 is a perspective, partially cross-section view of the FIG. 6 structure following the deposition of a gate insulator thereover;

FIG. 8 is a perspective, partially cross-section view of the structure following the deposition of two layers of semiconductor material;

FIG. 9 is a perspective, partially cross-section view of the FIG. 8 structure after patterning of the layers of semiconductor material;

FIG. 10 is a perspective, partially cross-section view of the structure following the deposition of two layers of source/drain metallization;

FIG. 11 is a perspective, partially cross-section view of the structure following completion of the structure through the formation of a substantially planar surface;

FIG. 12 is a plan view of a portion of the structure;

FIG. 13 is a perspective, partially cross-section view of the structure following uniform removal of enough material from the structure to expose the support layer within an aperture in the subordinate layer;

FIG. 14 is a perspective, partially cross-section view of the FIG. 13 structure following etching of the support layer in the self-aligned openings in the subordinate layer; and

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FIG. 15 is a perspective, partially cross-section view of the structure following formation of a passivation layer over the structure.

DETAILED DESCRIPTION

In accordance with one embodiment of the present invention, an amorphous silicon thin film (TFT) field effect transistor (FET) may be fabricated. Various stages in the fabrication of such a device in accordance with the present invention are illustrated in FIGS. 1-14.

In FIG. 1, a substrate 12 has a uniform reference layer 18 disposed thereon. Reference layer 18 comprises first and second sublayers 14 and 16. For fabrication of a thin film transistor, the layer 18 constitutes the gate conductor while the substrate 12 constitutes a larger structure on which the transistor is to be disposed. In many applications such as liquid crystal displays and imagers, it is desirable that the substrate 12 be transparent, however, transparency of the substrate is unimportant to the present process and thus, is a matter of design choice in accordance with the intended use of the thin film transistor to be fabricated. Typical transparent substrate materials are glass, quartz and appropriate plastics.

The gate conductor sublayers 14 and 16 are deposited on the substrate in sequence by any appropriate technique such as sputtering, chemical vapor deposition, thermal evaporation and so forth. This gate conductor is comprised of two layers of different metals such as a first layer of titanium disposed in contact with the substrate with a layer of molybdenum or aluminum (referred to as Mo/Ti and Al/Ti metallization, respectively) disposed thereover or a layer of chromium disposed on a substrate with a layer of molybdenum disposed thereover (Mo/Cr metallization). As a further alternative, the first sublayer of the gate conductor may be a transparent conductor material such as indium tin oxide or other transparent conductors. We prefer to use Mo/Cr.

The gate electrode is typically deposited to a thickness of 1,000 Å to 10,000 Å, depending on the sheet resistivity required for the gate electrode structure and the vertical height of the top hat gate required to achieve good self-alignment. With a Mo/Cr gate conductor, the Cr is preferably 100 to 500 Å thick and the Mo is preferably 1000 to 10,000 Å thick.

The FIG. 1 structure is then photomasked to provide a mask pattern corresponding to the desired gate conductor configuration as shown in FIG. 2. The upper surface of the second conductor 16 is exposed in the window 22 where the photoresist 20 has not been retained. Next, the structure is dry etched preferably using reactive ion etching to pattern the upper conductor layer 16 in accordance with the retained photoresist pattern. To do this, the wafer is mounted in a reactive ion etching apparatus which is then purged and evacuated in accordance with normal reactive ion etching procedures. A source gas flow preferably of 37.5 sccm (standard cubic centimeters per minute) of sulphur hexafluoride (SF₆), 6.5 sccm of Cl₂ and 16 sccm of O₂ is established, introduced into the etching chamber at a pressure of 65 mtorr and reactive ion etching potentials are applied to etch the molybdenum in the windows 22. This etching is preferably carried out until all the molybdenum is removed in center of the windows and is allowed to proceed for 40 seconds more of overetching to ensure that all of the molybdenum is removed from within the originally defined windows 22. This molyb-

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denum etching step is preferably carried out at a power of 200 watts.

Following this etching step, the structure appears as illustrated in FIG. 3. It will be noted, that the second conductor (molybdenum) has been removed from the structure everywhere outside the region which was initially protected by the retained portion of the photoresist 20. The original edges of the retained photoresist are indicated by the dash lines marked 22', but the photoresist has been etched back from that original edge as the etching of the molybdenum has proceeded. This results in the substantially 45° slope to the side walls of the molybdenum as illustrated in FIG. 3.

A tapered gate electrode of this type may be provided in a variety of other ways well known in the art including reliance on the erosion of the photoresist during etching of the gate conductor where reactive ion etching (RIE) is employed or an isotropic wet etch may be employed which undercuts the resist during etching of the unprotected portion of the gate conductor.

Such a slope is provided in RIE, in part because when the photoresist is baked after patterning to toughen it prior to RIE etching, the photoresist slumps with the result that its thickness tapers from small or zero at the edge of a photoresist region upward to the central thickness of the photoresist over a finite distance. During reactive ion etching, the photoresist erodes as the gate conductor is etched with the result that a taper is produced on the retained portion of the gate conductor.

Next, the etching gas is preferably changed to 70 sccm of Cl₂ and 30 sccm of O₂ at a pressure of 100 mtorr to remove the exposed chromium. This etch is preferably continued until all the exposed chromium appears to have been removed and is then continued for an additional 60 seconds to ensure complete removal of the exposed chromium. The degree of overetching which should be employed depends on the substrate composition and the relative etch rates of the first conductor 14 and the substrate in the etching composition employed. This etching step is preferably carried out at a power of 300 watts. Following this step, the structure appears as illustrated in FIG. 4.

Next, the molybdenum upper layer of the gate conductor is etched back to expose a desired width of the first gate conductor layer. This may be done with the RIE using the same source gases as for the initial etching of the molybdenum, provided that that etchant does not excessively etch the now exposed portion of the substrate where the chromium has been removed. Following this step, the structure appears as illustrated in FIG. 5.

The retained photoresist is then removed to leave the structure illustrated in FIG. 6.

Next, a gate dielectric layer 28 is deposited over the entire structure preferably by chemical vapor deposition or some other process which is known to produce a high integrity dielectric. This gate dielectric is preferably be silicon nitride but may be silicon dioxide or other dielectrics and is about 1,000 to 4000 Å thick. The chromium gate conductor layer 14 is sufficiently thin (10 to 1000 Å) and the sidewall of the molybdenum gate conductor layer 16 is sufficiently vertically inwardly tapered or sloped that a high integrity conformal dielectric layer results.

This deposition of gate dielectric on the upper surface of the structure is done in a conformal manner whereby the raised configuration of the patterned gate electrode extends to the upper surface of that gate dielectric layer,

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that is, the surface topography is essentially unchanged as shown in FIG. 7.

Thereafter, in the fabrication of a typical silicon thin film transistor, a layer 30 of intrinsic amorphous silicon is deposited on the gate dielectric layer in a conformal manner. This intrinsic amorphous silicon layer typically has a thickness on the order of 2,000 Å. A thinner layer 32 (about 500 Å) of doped (typically phosphorous doped, that is n+) amorphous silicon is then deposited on the intrinsic amorphous silicon in a conformal manner to provide the structure illustrated in FIG. 8.

The dielectric layer, the intrinsic amorphous silicon and the doped amorphous silicon may all be deposited in the same deposition chamber without breaking the vacuum. Where that is done, we prefer to stop the plasma discharge in the deposition chamber after the completion of the deposition of a particular layer until after the proper gas composition for the deposition the next layer has been established. We then re-establish the plasma discharge to deposit that new layer. Alternatively, the two silicon depositions may be done in different chambers.

At this stage, the silicon layers may be patterned photolithographically to restrict them to the part of the structure where the silicon is needed, as shown in FIG. 9.

Thereafter, the source/drain metallization is deposited over the structure in a conformal manner. In accordance with application Ser. No. 07/593,419, entitled, "Thin Film Transistor Structure With Improved Source/Drain Contacts", this source/drain metallization is preferably a two layer molybdenum on chromium (Mo/Cr) metallization in which the Cr is 100 to 1000 Å thick and the molybdenum is 1000 to 10,000 Å thick, as shown in FIG. 10. Alternatively, this metallization may be a single metal such as molybdenum, chromium or tungsten. Following this step, the structure appears as illustrated in FIG. 10.

A planarization layer 40 (which may be photoresist) is then formed over the entire structure to provide a substantially planar upper surface of the structure as shown in FIG. 11.

In this manner, the topology of the patterned gate conductor is propagated upward through the various layers, at least through the support layer (the n+ doped amorphous silicon in this example) on which the source/drain metallization is disposed. That propagation of topography could be terminated by the source/drain metallization itself, but is at this time preferably terminated by a separate planarization layer because common metallization deposition processes are substantially conformal in nature and making the source/drain metallization conformal enables the final source and drain electrodes to be thicker.

The entire structure is then etched back in a non-selective manner by a planarization reactive ion etch. This planarization etch is preferably stopped once the molybdenum over the gate electrode has been exposed. That exposed molybdenum is then selectively etched with the remaining portion of the planarization layer serving as the etching mask to restrict that etching to the molybdenum which is over the gate electrode. This is followed by etching the now exposed chromium. As illustrated in FIG. 12, a self-aligned overlap between the source and drain electrodes and the gate electrode is produced. Alternatively, the planarization etch may be continued until the chromium layer of the source/drain metallization has been exposed. That exposed chromium

34 is then selectively etched to expose the doped silicon 32. As a still further alternative, the planarization etch can be continued until the doped silicon becomes exposed.

At this stage, the exposed doped silicon is removed by etching to leave only intrinsic silicon between the source and drain electrodes. This normally involves the removal of some, but not all of the intrinsic amorphous silicon in order to ensure that all of the doped amorphous silicon has been removed.

A key consideration is that the source/drain gap in the circle 60 in the top down view in FIG. 13 is disposed in proper alignment with the underlying gate electrode 18. Since the source/drain gap is defined by the self-aligned planarization method just described, control of the size of the source/drain gap and its location is independent of the alignment of the etching mask 52 which controls the pattern and location of the other portions of the boundary of the retained source/drain metallization.

If the silicon was not patterned previously it is usually necessary to remove excess silicon exposed after the removal of the source/drain metal. This etch is done with the source/drain mask still in place in order to protect the exposed silicon in the channel region.

The source and drain metallization is then patterned to provide the various desired segments of the source and drain metallization which connect to various devices and interconnect devices in a manner which is appropriate to the structure being fabricated. The etching of the pattern of the source/drain metallization may preferably be done in two stages using RIE with the appropriate source gases discussed above or it may be done by wet etching or other means. This yields the structure illustrated in FIG. 14.

Thereafter, a passivation layer 48 may be deposited on the upper surface of the structure as shown in FIG. 15. This passivation layer is known as a back channel passivation layer since its purpose is to passivate the back or the away-from-the-gate-metallization surface of the silicon to maximize the stability of the device characteristics of this thin film transistor. This passivation layer is typically about 2,000 Å thick and may be silicon dioxide, silicon nitride or other insulators such as polyimide.

Typically, the illustrated thin film transistor is only one of many such thin film transistors which are simultaneously fabricated on the same substrate.

While the semiconductor material in the just described embodiment is amorphous silicon, since that is the material presently in typical use for thin film transistors, it should be understood that this process is equally applicable to the use of other semiconductor materials or other forms of silicon. Further, while the gate dielectric layer has been described as being silicon nitride, it will be understood that more than one sublayer may be present in the gate dielectric layer and various sublayers may have different compositions and a single layer dielectric may be SiO₂ or other dielectric materials.

Other semiconductor materials which are presently used in an amorphous condition are germanium and cadmium selenide. This process technique is applicable to those amorphous silicon semiconductor materials and any others as well as being applicable to polycrystalline or even monocrystalline semiconductor materials where the underlying support structure supports the formation of such semiconductor layers.

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It will be recognized that the distance by which the upper gate layer 16 is setback from the edge of the lower gate layer 14 is controlled by the rate at which the upper gate layer etches back and the length of time for which that etch back is allowed to proceed. By appropriate control of the etch rate and time this setback can be varied over a substantial range, from a fraction of a micron to several microns or more as may be considered desirable in a particular device.

This provides the ability to controllably increase the degree of overlap between the gate electrode and the source and drain electrodes of self-aligned device produced in accordance with application Ser. No. 07/593,425, "Device Self-Alignment by Propagation of a Reference Structure's Topography". This technique is also applicable to the methods disclosed in related applications Ser. Nos. application Ser. No. 07/510,767, entitled, "Method for Photolithographically Forming a Self-Aligned Mask Using Back Side Exposure and a Non-Specular Reflecting Layer" and application Ser. No. 07/499,733, entitled, "Method for Fabricating a Self-Aligned Thin-Film Transistor Utilizing Planarization and Back-Side Photoresist Exposure", provided that the first gate metallization layer is made of a material which is transparent or sufficiently transmissive of the actinic light employed to expose the photoresist that the photoresist can be exposed through the lower, thin, gate conductor and shadowed by the thick gate conductor in their self-aligned processes which expose the photoresist by directing the exposing radiation through the substrate as a means of establishing the channel region gap between the source and drain electrodes in a self-aligned manner. Transmission of the exposing (UV) radiation through the first, thin gate conductor layer may be provided by use of a conductor layer which is transparent to that light frequency or alternatively, by use of gate metallization material which is opaque to that light frequency, but whose thickness is kept below about 100 Å whereby a substantial portion of the actinic radiation incident thereon passes therethrough.

In this alternative process, the gate metallization pattern is fabricated in the same manner as described above and the device fabrication carried out in the manner described above through the deposition of the layer of intrinsic amorphous silicon. Next, a layer of dielectric material is deposited on that amorphous silicon layer. Then a positive photoresist layer is disposed on that layer of dielectric material, exposed to actinic radiation through the substrate and the underlying layers of the device being fabricated and developed. This leaves a plug of photoresist in alignment with the thick, upper conductor of the gate metallization. This plug is then used as a mask for the removal of the dielectric layer where it is not protected by the photoresist. This leaves a plug of the dielectric material disposed on the intrinsic amorphous silicon in alignment with the thick, upper gate conductor material. Since this plug is set back from the edge of the gate electrode (the outer edge of the lower thin gate conductor) and will eventually space between the source and drain electrodes and the gate is substantially greater than it is in those basic processes for the same photoresist exposure and development conditions. Consequently, there will in general be no need to overexpose or overdevelop the photoresist in order to increase that overlap between the gate electrode and the source and drain electrodes.

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Next, a layer of n⁺ doped amorphous silicon is deposited over the dielectric plug and the exposed portions of the intrinsic amorphous silicon. The source/drain metallization is then deposited, a planarization layer such as photoresist is formed over the upper surface of the structure and that upper surface of the structure is uniformly etched in a non-selective manner until the source/drain metallization is exposed over the dielectric plug because of its greater height there. This exposed portion of the source/drain metallization may then be selectively etched to expose the n⁺ doped amorphous silicon which is disposed on the dielectric plug. The now exposed portion of the n⁺ amorphous silicon is then removed to expose the top of the dielectric plug to isolate the source and drain electrodes from each other in this region. The source/drain metallization layer is then further patterned to remove at least those portions which connect the source and drain electrodes to each other outside this portion of the structure. Alternatively, that patterning of the source/drain metallization may be done before deposition of the planarization layer. Any other steps necessary to the fabrication of the device are then carried out.

There are a number of other variations possible. The silicon could be left unpatterned. This results in intrinsic amorphous silicon and n⁺ amorphous silicon being left under the source/drain metallization in all places. For applications such as imagers this is acceptable. Just the intrinsic amorphous silicon could be patterned before the n⁺ amorphous silicon deposition and then the source/drain metallization deposited. This would result in n⁺ under the source/drain metallization in all places. This could be acceptable even for displays where the contact to the transparent electrode would then be metal/n⁺/transparent electrode.

While the invention has been described in detail herein in accord with certain preferred embodiments thereof, many modifications and changes therein may be effected by those skilled in the art. Accordingly, it is intended by the appended claims to cover all such modifications and changes as fall within the true spirit and scope of the invention.

What is claimed is:

1. A method of fabricating a thin film transistor comprising the steps of:

depositing a first gate conductor layer on a major surface of a substrate;

depositing a second gate conductor layer over said first gate conductor layer, said second gate conductor layer being susceptible to etching under conditions under which said first gate conductor layer is substantially immune to etching;

providing a photoresist layer over said second gate conductor layer;

exposing and developing said photoresist in a pattern in accordance with a desired configuration of said first gate conductor layer;

etching said second gate conductor layer and said first gate conductor layer where they are not protected by the retained portion of said photoresist layer; then

etching back, with an etchant to which said first gate conductor layer is substantially immune, said second gate conductor layer to expose peripheral portions of said first gate conductor layer in a self aligned manner so as to form a patterned gate electrode having a gate conductor topology wherein said second gate conductor layer has sloped side-

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walls set back a selected overlap distance from sidewalls of said first gate conductor layer, said selected overlap distance corresponding to the exposed peripheral portions of said first gate conductor layer;

removing any remaining photoresist;

depositing over said substrate and said first and second gate conductor layers a substantially conformal gate dielectric layer, depositing over said gate dielectric layer a substantially conformal semiconductor material layer, and depositing over said semiconductor material layer a substantially conformal source/drain metallization layer such that said gate conductor topography is propagated upward through each of said layers;

applying a planarization layer over said source/drain metallization layer;

planarizing said planarization layer to expose at least a portion of said source/drain metallization layer disposed over and corresponding to an uppermost portion of said patterned gate conductor topography; and

etching said source/drain metallization layer to form self-aligned source and drain electrodes disposed over said first gate conductor layer at least by said selected overlap distance.

2. The method recited in claim 1 wherein said first gate conductor layer is substantially transparent to at least one frequency in the infrared-to-ultraviolet portion of the electromagnetic spectrum.

3. The method recited in claim 1 wherein: said semiconductor material is silicon.

4. The method recited in claim 1 wherein: said semiconductor material is amorphous silicon.

5. A method of fabricating a thin film transistor comprising the steps of:

depositing a first gate conductor layer on a major surface of a substrate;

depositing a second gate conductor layer over said first gate conductor layer, said second conductor being susceptible to etching under conditions under which said first gate conductor layer is substantially immune to etching;

providing a photoresist layer over said second gate conductor layer;

exposing and developing said photoresist in a pattern in accordance with a desired configuration of said first gate conductor layer;

etching said second gate conductor layer and said first gate conductor layer where they are not protected by the retained portion of said photoresist layer; then

etching back, with an etchant to which said first gate conductor layer is substantially immune, said second gate conductor layer to expose peripheral portions of said first gate conductor layer in a self-aligned manner so as to form a patterned gate electrode having a gate conductor topology wherein said second gate conductor layer has sloped sidewalls set back a selected overlap distance from sidewalls of said first gate conductor layer, said selected overlap distance corresponding to the exposed peripheral portions of said first gate conductor layer;

depositing a substantially conformal dielectric layer over said patterned gate conductor and exposed portions of said substrate upper surface;

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depositing a substantially conformal layer of semiconductor material over said dielectric layer;

depositing a layer of source/drain metallization over said semiconductor material layer;

forming a planarization layer of a planarization material over the source/drain metallization, said planarization layer having a substantially planar exposed surface;

uniformly removing said planarization material until said source/drain metallization is exposed in alignment with raised portions of said second gate conductor layer; and

selectively removing the exposed source/drain metallization to expose the underlying semiconductor material layer such that the remaining source/drain metallization is disposed over said patterned gate conductor by at least said selected overlap distance.

6. The method recited in claim 5 wherein: the step of depositing the layer of semiconductor material comprises:

first depositing a layer of substantially undoped semiconductor material; and

second depositing a layer of doped semiconductor material; and

said method further comprises, after the step of selectively removing the source/drain metallization, the step of:

removing the doped semiconductor material portion of said semiconductor material layer.

7. The method recited in claim 6 wherein: said semiconductor material is silicon.

8. The method recited in claim 7 wherein: said semiconductor material is amorphous silicon.

9. The method recited in claim 5 wherein: said semiconductor material is silicon.

10. The method recited in claim 9 wherein: said semiconductor material is amorphous silicon.

11. The method recited in claim 5 further comprising the step of:

providing a back channel passivation layer over the structure.

12. The method recited in claim 5 wherein said first gate conductor layer is substantially transparent to at least one frequency in the infrared-to-ultraviolet portion of the electromagnetic spectrum.

13. A method of fabricating a thin film transistor comprising the steps of:

depositing a first gate conductor layer on a major surface of a substrate, said first gate layer being transmissive of at least one frequency of radiation capable of exposing photoresist;

depositing a second gate conductor layer over said first gate conductor layer, said second conductor layer being opaque to said at least one frequency of radiation and being susceptible to etching under conditions under which said first gate conductor layer is substantially immune to etching;

providing a photoresist layer over said second gate conductor layer;

exposing and developing said photoresist in a pattern in accordance with a desired configuration of said first gate conductor layer;

etching said second gate conductor layer and said first gate conductor layer where they are not protected by the retained portion of said photoresist layer; then

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etching back, with an etchant to which said first gate conductor layer is substantially immune, said second gate conductor layer to expose peripheral portions of said first gate conductor layer in a self-aligned manner so as to form a patterned gate electrode having a gate conductor topology wherein said second gate conductor layer has sloped sidewalls set back a selected overlap distance from sidewalls of said first gate conductor layer, said selected overlap distance corresponding to the exposed peripheral portions of said first gate conductor layer;

depositing a first substantially conformal dielectric layer over said patterned gate conductor and exposed portions of said substrate upper surface;

depositing a substantially conformal layer of semiconductor material on said dielectric layer;

depositing a second layer of photoresist on the second dielectric layer;

exposing a back-side substrate surface, opposite to said major substrate surface, to UV light for a selected duration, to cause exposure of at least a portion of the second photoresist layer outside of a shadow of the opaque portion of said gate electrode;

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removing at least the exposed second photoresist portion by selective development, to form a mask for etching the second dielectric layer;

etching said second dielectric layer to remove the portions not protected by the retained portion of said second photoresist;

depositing a layer of doped semiconductor material on the exposed semiconductor portion and over the remaining portion of the second dielectric layer;

depositing a layer of source/drain metallization over said doped semiconductor material layer;

forming a planarization layer of a planarization material over the source/drain metallization, said planarization layer having a substantially planar exposed surface;

uniformly removing said planarization material until said source/drain metallization is exposed in alignment with raised portions of said patterned gate conductor; and

selectively etching the exposed portion of the source/drain metallization and a portion of the doped semiconductor layer, to expose at least a top surface of the remaining portion of said second dielectric layer, and to form self-registered source and drain electrodes each of which overlaps the gate electrode at least by said selected overlap distance.

* * * * *

EXHIBIT 7

United States Patent [19] Miyago et al.

[11] Patent Number: **5,036,370**
[45] Date of Patent: **Jul. 30, 1991**

[54] **THIN FILM SEMICONDUCTOR ARRAY
DEVICE**

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[73] Assignee: **Sharp Kabushiki Kaisha, Japan**

[21] Appl. No.: **545,955**

[22] Filed: **Jul. 2, 1990**

[30] **Foreign Application Priority Data**

Jul. 4, 1989 [JP] Japan 1-173783

[51] Int. Cl.⁵ **H01L 27/12; H01L 27/01;
H01L 29/78; H01L 23/48**

[52] U.S. Cl. **357/4; 357/23.7;
357/23.15; 357/71**

[58] Field of Search **357/4, 23.7, 23.1, 71,
357/23.15**

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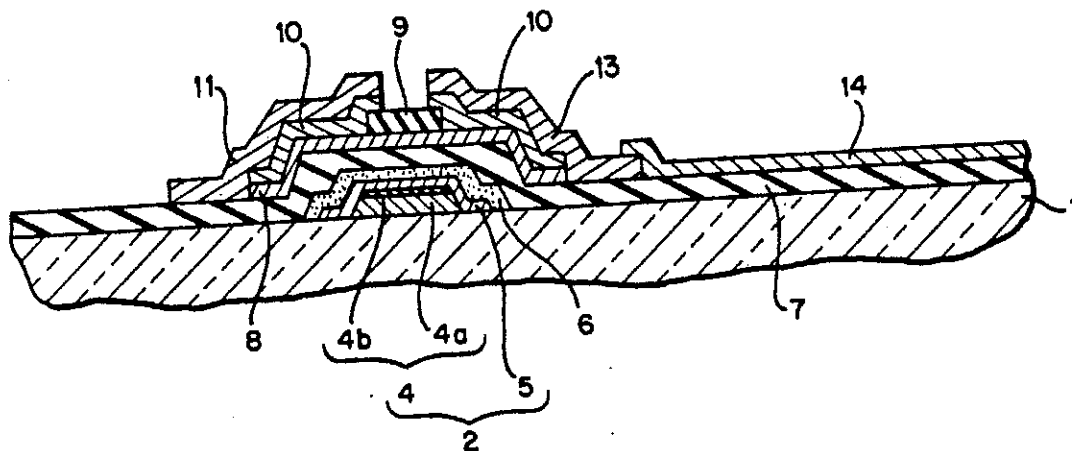
62-80626 4/1987 Japan .

Primary Examiner—Mark Prenty
Attorney, Agent, or Firm—Nixon & Vanderhye

ABSTRACT

[57] The production of a thin film transistor array device having a gate wiring on an insulated substrate. The gate wiring has an inner gate wiring having a first metal layer formed on the insulated substrate and a second metal layer whose etching speed is faster than that of the first metal layer, the first metal layer and the second metal layer being overlapped so as to constitute a dual structure, and an outer gate wiring covering the inner gate wiring.

3 Claims, 4 Drawing Sheets

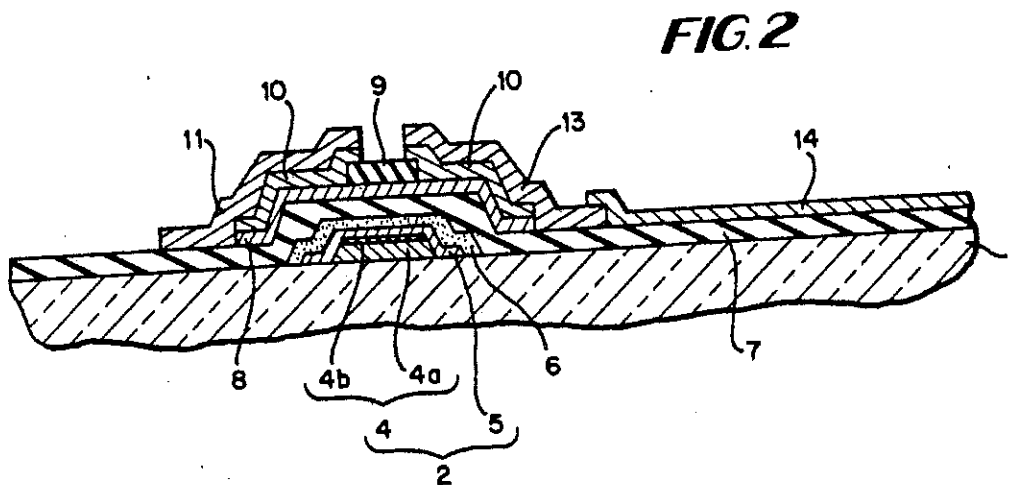
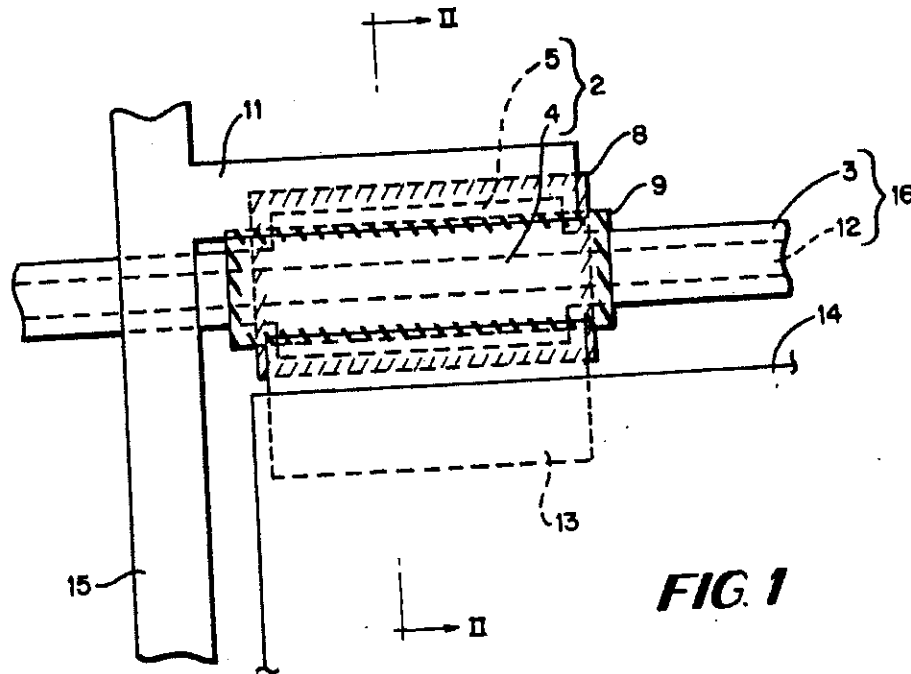


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FIG. 3A

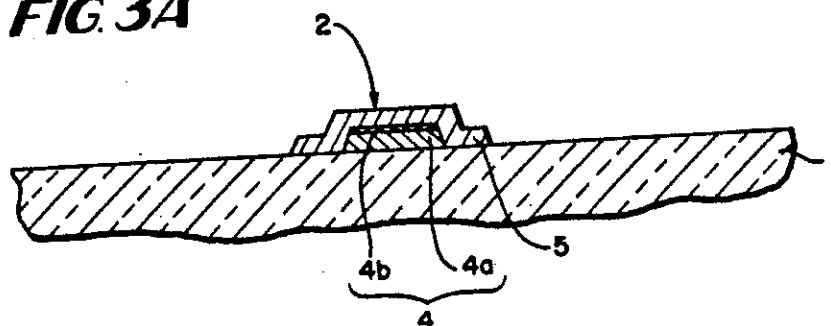


FIG. 3B

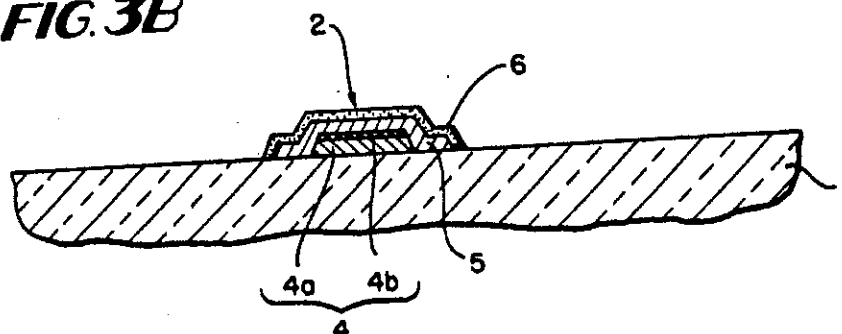
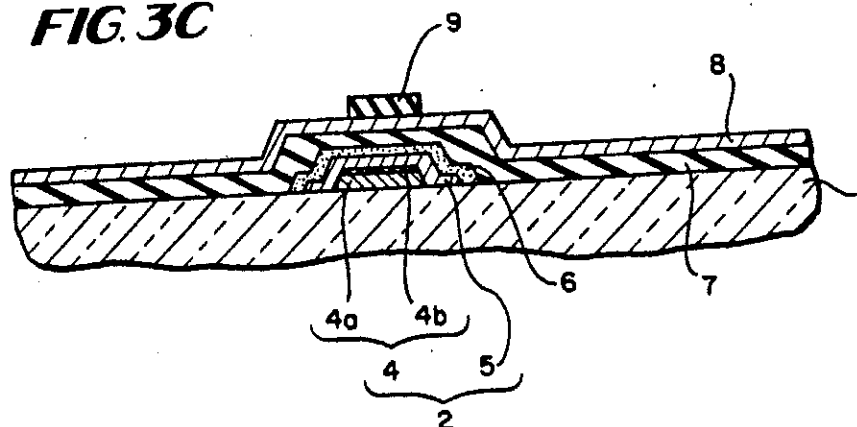


FIG. 3C



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FIG. 3D

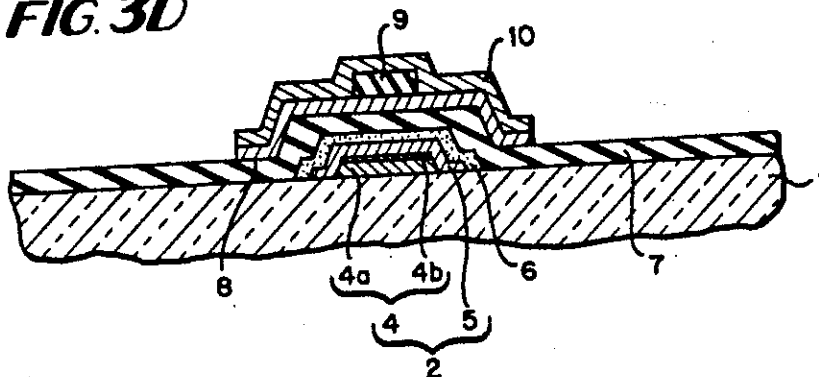


FIG. 3E

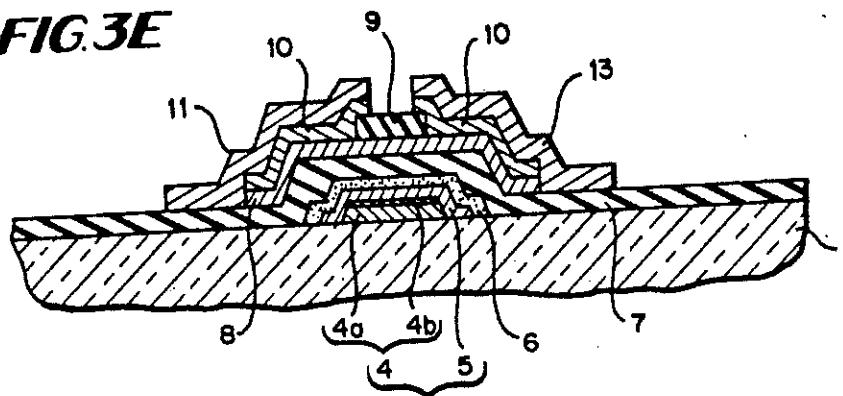
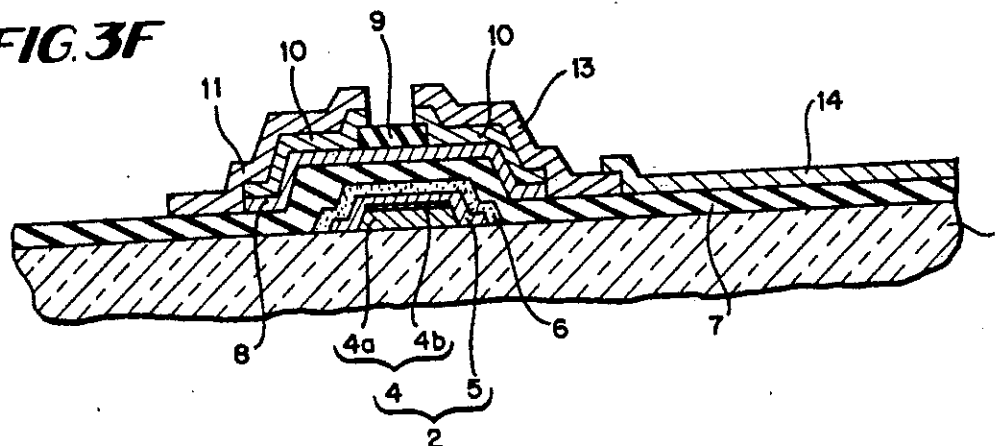


FIG. 3F



U.S. Patent

July 30, 1991

Sheet 4 of 4

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FIG. 4

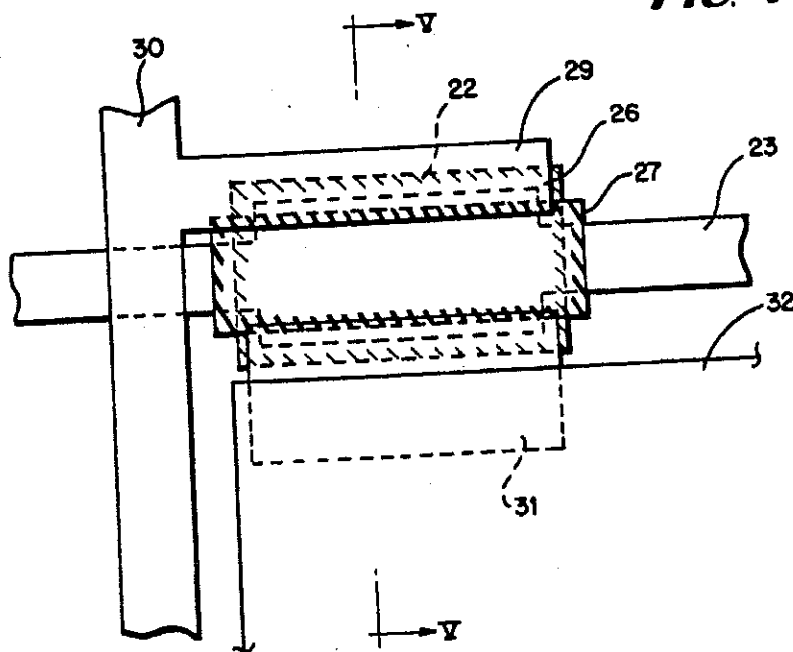


FIG. 5

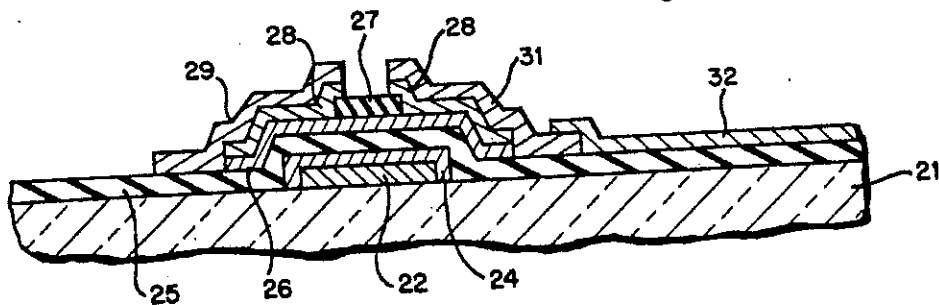
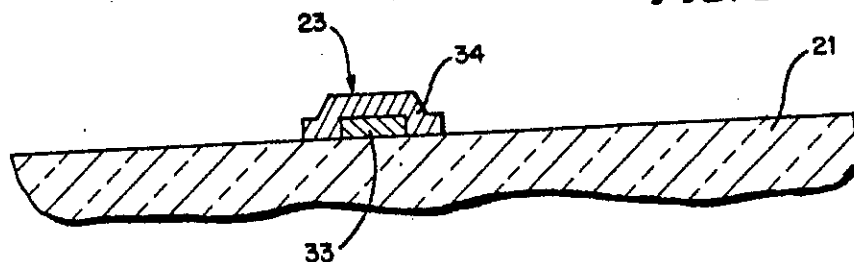


FIG. 6



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THIN FILM SEMICONDUCTOR ARRAY DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to a transistor array device, and a method for producing the same. More particularly, the present invention relates to a thin film transistor array device adapted for use in large-screen active matrix display devices and a method for producing the same. Hereinafter, the thin film transistor will be referred to as "TFT".

2. Description of the Prior Art

Liquid crystal display devices which employ an active matrix system having a TFT array formed on an insulated substrate so as to drive picture element electrodes through the TFT are well known. The active matrix system has an advantage in that it can be applied to display devices designed to display on a large-scale screen with high density, whether the display is to be a reflecting type or a permeating type.

To obtain the TFT arrays, amorphous silicone (hereinafter referred to as "a-Si") or polycrystalline silicone is used as semiconductor material. FIG. 4 shows a conventional TFT array in which the rim of the layered portions is hatched with the central portion remaining unhatched for simplicity.

Referring to FIG. 5, the conventional fabrication of a TFT array device will be described:

Tantalum (Ta) is deposited on a glass substrate 21 by a sputtering method to a thickness of 3,000 to 4,000 Å, and gate wirings 23 are formed in patterns by a photolithography or by an etching method. The gate wirings 23 can be formed by a lift-off method. A wider portion of the gate wiring 23 functions as a gate electrode 22. The surfaces of the gate electrode 22 and the gate wirings 23 are anodized so as to form an anodized film 24 which functions as a gate insulator film.

Subsequently, the anodized glass substrate 21 is covered with a gate insulating film 25, to the thickness of 2,000 to 4,000 Å containing silicon nitride (hereinafter referred to as "SiNx") by a plasma activated chemical vapor deposition method (hereinafter referred to as plasma CVD method).

The gate insulator film 25 is covered with an a-Si(i) layer (150 to 1,000 Å thick) and then with a SiNx layer (100 to 2,000 Å thick). The a-Si layer later becomes a semiconductor layer 26, and the SiNx layer later becomes an insulator layer 27. Subsequently, the SiNx layer is formed in a desired pattern, and an insulator layer 27 is formed on a portion of the gate electrode 22 except for the outer part thereof.

The insulator layer 27 on the glass substrate 21 is covered with an a-Si(n+) layer (300 to 2,000 Å thick) doped with phosphorus, which layer becomes a contact layer 28 by a plasma CVD. Finally, the a-Si(i) layer and the a-Si(n+) layer are formed in a desired pattern to form the semiconductor layer 26, and the contact layer 28 which is continuous on the insulator layer 27 at this stage.

A metal film of Mo, Ti, Al or the like is formed to the thickness of 2,000 to 10,000 Å on the glass substrate 21 so as to cover the semiconductor layer 26 and the contact layer 28, and the metal film is formed in pattern by etching so that a source electrode 29, a source bus 30 and a drain electrode 31 are formed. In this way a TFT is formed. The contact layer 28 is also subjected to the etching on insulator layer 27, thereby separating into a

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first portion under the source electrode 29 and a second portion under the drain electrode 31. Finally, the source electrode 29, the source bus 30 and the drain electrode 31 are entirely covered with an indium tin oxide (ITO) film by sputtering. The ITO film is formed in a desired pattern to form a picture element electrode 32.

Such TFTs are formed in plurality on the gate wiring 23 to form the TFT array. The source bus 30 is perpendicular to the extension of the gate wiring 23, and is connected to the respective source electrodes 29 of the TFTs.

In the active matrix display device employing the TFT arrays the scanning signals are consecutively input to the gate wiring 23, and picture element signals are input to the source bus 30 to drive the picture element electrode 32. The gate wiring 23 and the source bus 30 have 307,200 junctions in a display device having picture elements of 480×640. If leak occurs at one of these picture elements between the gate wiring 23 and the source bus 30, a cross-type line failure occurs. This line failure spoils the quality of the image, and reduces the efficiency of the display device.

In the known display device described above, Ta is used for the gate wiring 23 because of its capability of being coated with an anodized film 24 whereby the gate wiring 23 and the source bus 30 are insulated. When the gate wiring 23 is made of Ta, an advantage is that the gate wiring 23 has a smooth tapered side, which prevents the source bus 30 from breakage at its junctions.

On the other hand, a disadvantage is that in a large-scale display device having a long gate wiring 23, the scanning signals attenuate because of Ta having a large specific resistance. As a result, the brightness of picture elements are different between two points adjacent to the input section of the signals and remote from the input section, thereby resulting in the detrimental brightness gradient in picture elements spreading from the input section.

In order to solve such problems, one proposal shown in FIG. 6 is that the gate wiring has a dual layer structure, that is, an inner gate wiring 33 of metal having low specific resistance such as Al, Al-Si, or Al-Si-Cu, and an outer gate wiring 34 of the Ta. The advantage of this structure is that the inner gate wiring 33 avoids the undesired production of brightness gradient.

To prevent leaks from occurring at a junction by use of gate wirings 23 having the dual layer structure, it is essential to completely cover the inner gate wiring 33 with the outer gate wiring 34. This is because in the process of forming the outer gate wiring 34 of Ta in pattern by etching, the etching speed of Al and other metals is higher than the etching speed of Ta. However, the inner gate wiring 33 of Al, Al-Si, or Al-Si-Cu cannot be formed so as to have a smooth inclined side. The rough sides are likely to cause the outer gate wiring 34 overlaying the inner gate wiring 33 to break. If the outer gate wiring 34 is broken in this way, the coverage of the inner gate wiring 33 fails. In addition, in the process of removing the resist after the inner gate wiring 33 is formed, the inner gate wiring 33 is liable to hillocks and voids. If the hillocks and voids occur on the inner gate wiring 33, its complete coverage becomes impossible. This causes leaks between the gate wiring 23 and the source bus 30 regardless of the existence of a gate insulating film 25.

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SUMMARY OF THE INVENTION

The transistor array device of the present invention, which overcomes the above-discussed and numerous other disadvantages and deficiencies of the prior art, comprises a gate wiring on an insulated substrate, the gate wiring comprising an inner gate wiring having a first metal layer formed on the insulated substrate and a second metal layer whose etching speed is faster than that of the first metal layer, the first metal layer and the second metal layer being overlapped so as to constitute a dual structure, and an outer gate wiring covering the inner gate wiring.

In a preferred embodiment, the inner gate wiring has a smaller specific resistance than that of the outer gate wiring.

In another preferred embodiment, the outer gate wiring is covered with an anodizing film.

According to another aspect of the present invention, there is provided a process for constructing a thin film transistor array device having a gate wiring on an insulated substrate, the process comprising the steps of overlapping a first metal layer over a second metal layer whose etching speed is faster than that of the first metal layer, forming an inner gate wiring in pattern on the first and second metal layers, and covering the inner gate wiring with an outer gate wiring.

In a preferred embodiment, the process further comprises a step of forming an anodized film on the outer gate wiring.

Thus, the invention described herein achieves the objects of (1) providing a thin film transistor array device having a gate wiring capable of anodizing, thereby reducing the specific resistance of the gate wiring, and (2) providing a thin film transistor array device capable of enhancing the image quality when it is applied to a large-screen display, thereby, increasing the efficiency of the display device and reducing the production cost.

BRIEF DESCRIPTION OF THE DRAWINGS

This invention may be better understood and its numerous objects and advantages will become apparent to those skilled in the art by reference to the accompanying drawings as follows:

FIG. 1 is a plan view showing a transistor array device according to the present invention;

FIG. 2 is a cross-sectional view taken along the line II-II in FIG. 1;

FIGS. 3A to 3F are cross-sectional views explaining the steps of constructing the transistor array device of FIG. 1;

FIG. 4 is a plan view showing a conventional TFT semiconductor array device;

FIG. 5 is a cross-sectional view taken along the line V-V line in FIG. 4; and

FIG. 6 is a cross-sectional view showing an modified example of the gate wiring.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIGS. 1, 2 and 3A-3F, and Al layer 4a (1,000 Å thick), and an Mo layer 4b (500 Å thick) were consecutively deposited on a glass substrate 1 by a sputtering method. A desired shape of etching mask was formed on the Mo layer 4b with a photo resist film, and etching was carried out in accordance with the etching mask so that an inner gate wiring 12 was formed as shown in FIG. 1. A part of the inner gate wiring 12 is

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used as an inner gate electrode 4. Each of the inner gate wiring 12 and the inner gate electrode 4 has a width of 15 μm.

Subsequently, a Ta layer (3,000 Å thick) was deposited on the Mo layer 4b, and an outer gate wiring 3 and an outer gate electrode 5 were formed in pattern, each of which had a greater width by 1 μm or more than those of the inner tape wiring 12 and the inner gate electrode 4 (FIG. 3A). A rim portion of the outer gate wiring 3 is used as the outer gate electrode 5. In the illustrated example the inner gate wiring 12 and the outer gate wiring 3 constitute the gate wiring 16. Likewise, inner gate electrode 4 and the outer gate electrode 5 constitute the gate electrode 2.

The top surfaces of the outer gate electrode 5 and the outer gate wiring 3 were anodized so as to form an anodized film 6 consisting of Ta₂O₅ and functioning as a gate insulating film as shown in FIG. 3B. Since the Ta₂O₅ film is resistant to etching, it protects the outer gate electrode 5, the outer gate wiring 3, the inner gate wiring 12 and the inner gate electrode 4 against an etchant used in a later etching for forming TFTs.

The entire surface of the glass substrate 1 was covered with a gate insulating film 7 (4,000 Å thick) consisting of SiNx by a plasma CVD method. the gate insulating film 7 is covered with an a-Si(i) layer (300 Å thick) which later becomes a semiconductor layer 8, and a SiNx layer (2,000 Å thick) which later becomes an insulating layer 9 in this order. The SiNx layer was formed in a desired pattern, and the insulating layer 9 was formed only above the gate electrode 2 (FIG. 3C).

The glass substrate 1 and the insulating layer 9 thereon was covered with an a-Si(n⁺) layer (1,000 Å thick) by a plasma CVD method. Then, the a-Si(i) layer and a-Si(n⁺) layer were formed in pattern so that semiconductor layer 8 and the contact layer 10 were formed (FIG. 3D). The contact layer 10 functions as an ohmic contact among the semiconductor layer 8, the source electrode 11 and the drain electrode 13. At this stage, the contact layer 10 is continuous on the insulating layer 9.

The entire surface of this glass substrate 1 was covered with a Ti layer (3000 Å thick) which was formed in pattern by etching to form the source electrode 11 and the drain electrode 13. At this stage, the contact layer 10 on the insulating layer 9 was removed by etching, thereby separating into two portions below the source electrode 11 and the drain electrode 13 (FIG. 3E). The source wiring 15 crossing the gate wiring 16 was formed at this time. In this way, the TFT array device is obtained.

Subsequently, the entire surface of the glass substrate 1 was covered with an ITO film by sputtering. The ITO film was formed in a desired pattern, thereby forming a picture element electrode 14 (FIG. 3F). In this way an active matrix substrate is formed.

The TFT array device of the present invention has a gate wiring 16 which includes an inner gate wiring 12 having an Al layer 4a and an Mo layer 4b overlapped in this order, and an outer gate wiring 3 of Ta covering the inner gate wiring 12. Because of the small specific resistance of the gate wiring 16 which is composed of the Al layer 4a and the Mo layer 4b, the picture elements which are represented by the picture element electrode 14 connected to the same gate wiring 16 are prevented from a detrimental brightness gradient.

Since the inner gate wiring 12 is constituted with a dual layer having the Al layer 4a and the Mo layer 4b

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overlapped, the Al layer 4a is protected from hillocks and voids. In addition, since the etching speed at which the Mo layer 4b forms the inner gate wiring 12 and the inner gate electrode 4 is faster than that by the Al layer 4a with respect to the etchant, the cross-section of the inner gate wiring 12 becomes tapered by its width becoming smaller progressively from the glass substrate 1.

Since the outer gate wiring 3 is wider than the inner gate wiring 12, the tapered inner gate wiring 12 is completely covered with the outer gate wiring 3. Owing to the coverage the inner gate wiring 12 is kept safe from an etching liquid. After the outer gate wiring 3 is formed and its surface is covered with the anodized film 6, the gate wiring 16 has a tapered side, thereby ensuring that the source wirings 15 crossing the gate wiring 16 are kept safe from breakage.

As described above, the gate electrode 2 is protected from breakage because of its smooth side surface and smooth top surface like the gate wiring 16. A TFT layer 8 overlaid thereon through a gate insulating film is also protected from detrimental breakage. Thus, the TFT layer 8 can be made thin without trading off the effectiveness. Thin TFT semiconductor layers 8 increase resistance during the gate-off period. A large gate-off resistance maintains the potential of the picture element electrode 14 at a high level until a subsequent scanning signal is input.

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It is understood that various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of this invention. Accordingly, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be construed as encompassing all the features of patentable novelty that reside in the present invention, including all features that would be treated as equivalents thereof by those skilled in the art to which this invention pertains.

What is claimed is:

1. A thin film transistor array device having a gate wiring on an insulating substrate, the gate wiring comprising an inner gate wiring having a first metal layer formed on the insulating substrate and a second metal layer whose etching speed is faster than that of the first metal layer, the first metal layer and the second metal layer being overlapped so as to constitute a dual structure, and an outer gate wiring covering the inner gate wiring.

2. A thin film transistor array device according to claim 1, wherein the inner gate wiring has a smaller specific resistance than that of the outer gate wiring.

3. A thin film transistor array device according to claim 1 or 2, wherein the outer gate wiring is covered with an anodized film.

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EXHIBIT 8

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ISSUE CLASSIFICATION	

U.S. UTILITY Patent Application

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PATENT DATE
JUN 03 2003

PATENT NUMBER

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APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/983629	D F	257 438	149	2815/18	P. DANG

Hyun-Sik Seo

Thin-film transistor and method of making same

PTO-2040
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ISSUING CLASSIFICATION			
ORIGINAL		CROSS REFERENCE(S)	
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438	149	438	937
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<input type="checkbox"/> TERMINAL DISCLAIMER <input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed. <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____ <input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	DRAWINGS Sheets Drawn: 89 Figs. Drawn: 20 Print Figs.: 6E			CLAIMS ALLOWED Total Claims: 15 Print Claim for O.G.: 1	
	PHUC T. DANG 1/19/03 (Assistant Examiner) David Helges Supervisory Patent Examiner Technology Center 2800 (Primary Examiner) M. Bauman 1/24/03 (Legal Instruments Examiner)			NOTICE OF ALLOWANCE MAILED 123-03 ISSUE FEE (W) Amount Due: 1600 Date Paid: 4-23-03 ISSUE BATCH NUMBER	

WARNING:

The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 422, 423 and 398. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

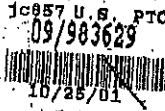
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Formal Drawings (9 sheets) set

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CONTENTS

	Date Received (Incl. C. of M.) or Date Mailed	Date Received (Incl. C. of M.) or Date Mailed
1. Application papers.	10/25/01	42.
2. <u>LOS</u>	10/25/01	43.
3. <u>priority</u>	10/25/01	44.
4. <u>Amend A</u>	10/25/01	45.
5. <u>Rejection (3 months)</u>	8/14/02	46.
6. <u>Amend B</u>	11-13-02	47.
7. <u>Drawing change</u>	11-13-02	48.
8. <u>PTOL 37</u>	1/23/03	49.
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POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	<i>Shinnell</i>		10-25-09
O.I.P.E. CLASSIFIER		535	01/15/02
FORMALITY REVIEW	<i>CB</i>		
RESPONSE FORMALITY REVIEW			

INDEX OF CLAIMS

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N Non-elected
 I Interference
 A Appeal
 O Objected

Claim	Date
Final Original	
1	1/14/02
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IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: Hyun-Sik SEO Conf.: 1252
Serial No.: 09/983,629 Art Unit: 2818
Filed: October 25, 2001 Examiner: P. Dang
For: THIN FILM TRANSISTOR AND METHOD OF MAKING
SAME

AMENDMENT UNDER 37 C.F.R. §1.111

Assistant Commissioner for Patents
Washington, DC 20231

November 13, 2002

Sir:

In response to the Office Action dated August 14, 2002 (Paper No. 5), the following amendments and remarks are respectfully submitted in connection with the above-identified application:

IN THE CLAIMS:

Please amend claims 11, 16, 20, and 26 as follows:

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11. (Amended) A method of making a thin-film transistor, comprising the steps of:
- depositing a first metal layer, formed of a metal exhibiting tensile stress, on a substrate;
- depositing a second metal layer, formed of a material exhibiting compressive stress, on the first metal layer directly after the step of depositing the first metal layer;

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Page 2

forming a single photoresist having a predetermined width on the second metal layer;
patterning the second metal layer using the single photoresist as a mask;
patterning the first metal layer using the photoresist as a mask, the first metal layer
31 *encl.* being etched to have a width greater than a width of the second metal layer, wherein the
second metal layer is formed only on a portion of the first metal layer, leaving two side
portions on a horizontal upper surface of the first metal layer having no second metal layer
formed thereon, thus forming a gate having a laminated structure of the first and second
metal layers; and
removing the photoresist,
wherein the steps of patterning the second metal layer and the first metal layer each
comprises a single etching step.

B2 16. (Amended) The method of making a thin-film transistor as claimed in claim 15,
wherein the second metal layer is formed from Mo, an Mo alloy, MoTa, MoW or MoNb.

B3 20. (Amended) A method of making a thin-film transistor, comprising the steps of:
depositing a first metal layer on a substrate, the first metal layer exhibiting tensile
stress;
depositing a second metal layer on the first metal layer without forming a photoresist
on the first metal layer beforehand, the second metal layer exhibiting compressive stress;
forming a photoresist having a predetermined width on the second metal layer;
etching the first and second metal layers so that the first metal layer is wider than the
second metal layer, wherein the second metal layer is formed only on a portion of the first

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B3
concl. metal layer, leaving two side portions on a horizontal upper surface of the first metal layer having no second metal layer formed thereon, to form a gate electrode having a double-layered structure including the first and second metal layers;
removing the photoresist; and
forming a single gate insulating layer directly on at least one of the first and second metal layers such that the single gate insulating layer directly contacts at least one of the first and second metal layers.

B4 26. (Amended) A method of making a thin-film transistor, comprising the steps of:
depositing a first metal layer on a substrate, the first metal layer being formed of a metal exhibiting tensile stress;
depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand, the second metal layer being formed of metal exhibiting compressive stress;
forming a single photoresist having a predetermined width on the second metal layer;
patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, wherein the second metal layer is formed only on a portion of the first metal layer, leaving two side portions on a horizontal upper surface of the first metal layer having no second metal layer formed thereon; and
removing the photoresist.

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Amendment filed November 13, 2002
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REMARKS

Applicant thanks the Examiner for the thorough consideration given the present application.

Claims 11-26 are pending in this application. Claims 11, 20, and 26 are independent.

Claims 11, 16, 20, and 26 are amended.

Reconsideration of this application, as amended, is respectfully requested.

Priority Under 35 U.S.C. §119


Applicant thanks the Examiner for acknowledging the claim for foreign priority under 35 U.S.C. §119, and receipt of the certified copy of the priority document in the parent application.

Information Disclosure Statement

The Examiner has acknowledged receipt of the Information Disclosure Statement filed October 25, 2001, and has returned an initialed copy of the Form PTO-1449. No further action is necessary at this time.

Drawings

The Examiner indicates on page 3 of the Office Action that source electrode 42 is not shown in FIG. 3. Included with the accompanying Letter to the Official Draftsperson is a proposed change to FIG. 3, and revised formal drawing therefor, showing source electrode 42. In view of this change and the indication in the Office Action Summary that the formal drawings filed with the present application are approved, The Examiner is respectfully requested to



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Group Art Unit 2818

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Page 5

provide a Notice of Draftsperson's Patent Drawing Review, Form PTO-948, confirming this approval with the next official communication.

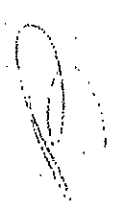
Claim Objection

Claims 16 and 20 are objected to as containing informalities. The dependency of claim 16 has been corrected. The informality of claim 20 has been corrected. Accordingly, reconsideration of the objection to the claims is requested.

Rejections under 35 U.S.C. §103(a)

Claims 11, 12, 14-20, 22-25, and 26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,235,561 to Seiki et al. Claims 13 and 21 are rejected as being unpatentable over Seiki et al. in view of U.S. Patent No. 6,300,152 to Kim. These rejections are respectfully traversed.

While not conceding the appropriateness of the Examiner's rejection, but merely to advance prosecution of the instant application, independent claims 11, 20 and 26 have been amended to recite combinations of method steps in a method of making a thin-film transistor including a "second metal layer ... formed only on a portion of the first metal layer, leaving two side portions on a horizontal upper surface of the first metal layer having no second metal layer formed thereon." Applicants respectfully submit that these combinations of method steps, as set forth in independent claims 11, 20 and 26, are not disclosed or made obvious by the prior art of record, including Seiki et al. or Kim.



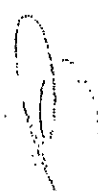
Serial No 09/983,629
Group Art Unit 2818

Attorney Docket No. 630-1536P
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In contrast to Applicant's claimed invention, Seiki et al. merely show depositing an aluminum film 110, a molybdenum film 112, and a photoresist 17 on a glass substrate 100, as shown in FIGS. 6a-6c. The layers are etched such that a third conductive molybdenum layer 113 is formed on an entire upper surface of the first conductive aluminum layer 111. Seiki et al. do not teach or suggest a second metal layer formed only on a portion of the first metal layer, leaving two side portions on a horizontal upper surface of the first metal layer having no second metal layer formed thereon, as set forth in the presently claimed invention.

In rejecting claims 13 and 21, the Office Action relies on Kim for teachings of forming a second insulating layer covering a semiconductor layer, a source electrode, a drain electrode and a first insulating layer. The effective filing date of the present application is August 26, 1997 since the present application is a divisional of U.S. Patent Application No. 08/918,462, now U.S. Patent No. 6,333,518. Because Kim's filing date of December 27, 1999, is later than the effective filing date of the present application, Kim cannot be used as prior art against the claims of the present application. Furthermore, Kim does not teach or suggest the above-cited features of claims 11 and 20, incorporated in claims 13 and 21 and, therefore, fails to cure the deficiencies of Seiki et al.

Applicants submit that claims 12-19 and 21-25 depend, either directly or indirectly, from independent claims 11 and 20, which are allowable for the reasons set forth above, and therefore claims 12-19 and 21-25 are allowable based on their dependence from claims 11 and 20. Reconsideration and allowance thereof are respectfully requested.



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Conclusion

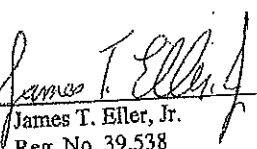
All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant, therefore, respectfully requests that the Examiner reconsider the outstanding objection and rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and that the present application is in condition for allowance.

If the Examiner believes for any reason that personal communication will expedite prosecution of this application, he is invited to telephone Sam Bhattacharya, Reg. No. 48,107, at (703) 205-8000.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

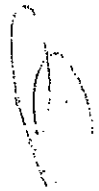
Respectfully submitted,
BIRCH, STEWART, KOLASCH & BIRCH, LLP

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MARKED-UP COPY OF AMENDMENTS

Claims 11, 16, 20, and 26 are amended as follows:

11. (Amended) A method of making a thin-film transistor, comprising the steps of:
- depositing a first metal layer, formed of a metal exhibiting tensile stress, on a substrate;
 - depositing a second metal layer, formed of a material exhibiting compressive stress, on the first metal layer directly after the step of depositing the first metal layer;
 - forming a single photoresist having a predetermined width on the second metal layer;
 - patterning the second metal layer using the single photoresist as a mask;
 - patterning the first metal layer using the photoresist as a mask, the first metal layer being etched to have a width greater than a width of the second metal layer, wherein the second metal layer is formed only on a portion of the first metal layer, leaving two side portions on a horizontal upper surface of the first metal layer having no second metal layer formed thereon, thus forming a gate having a laminated structure of the first and second metal layers; and
 - removing the photoresist[;],
- wherein the steps of patterning the second metal layer and the first metal layer each [comprise] comprises a single etching step.

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16. (Amended) The method of making a thin-film transistor as claimed in claim [9]
15, wherein the second metal layer is formed from Mo, [a] an Mo alloy, MoTa, MoW or
MoNb.

20. (Amended) A method of making a thin-film transistor, comprising the steps of:
depositing a first metal layer on a substrate, the first metal layer exhibiting tensile
stress;
depositing a second metal layer on the first metal layer without forming a photoresist
on the first metal layer beforehand, the second metal layer exhibiting compressive stress;
forming a photoresist having a predetermined width on the second metal layer;
etching the first and second metal layers so [such] that the first metal layer is wider
than the second metal layer, wherein the second metal layer is formed only on a portion of
the first metal layer, leaving two side portions on a horizontal upper surface of the first metal
layer having no second metal layer formed thereon, to form [agate] a gate electrode having a
double-layered structure including the first and second metal layers;
removing the photoresist; and
forming a single gate insulating layer directly on at least one of the first and second
metal layers such that the single gate insulating layer directly contacts at least one of the first
and second metal layers.

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26. (Amended) A method of making a thin-film transistor, comprising the steps of:
depositing a first metal layer on a substrate, the first metal layer being formed of a metal exhibiting tensile stress;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand, the second metal layer being formed of metal exhibiting compressive stress;

forming a single photoresist having a predetermined width on the second metal layer;

patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, wherein the second metal layer is formed only on a portion of the first metal layer, leaving two side portions on a horizontal upper surface of the first metal layer having no second metal layer formed thereon; and

removing the photoresist.

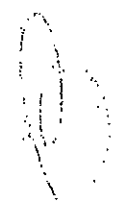


EXHIBIT 9



US007075595B2

(12) **United States Patent**
Moon

(10) **Patent No.:** **US 7,075,595 B2**
(45) **Date of Patent:** **Jul. 11, 2006**

(54) **LIQUID CRYSTAL DISPLAY DEVICE ARRAY
SUBSTRATE AND METHOD OF
MANUFACTURING THE SAME**

(75) **Inventor:** **Hong-Man Moon, Kumi-shi (KR)**

(73) **Assignee:** **LG. Phillips LCD Co., Ltd., Seoul (KR)**

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 446 days.

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(21) **Appl. No.:** **10/690,578**

(22) **Filed:** **Oct. 23, 2003**

(65) **Prior Publication Data**

US 2004/0080681 A1 Apr. 29, 2004

Related U.S. Application Data

(62) Division of application No. 09/867,484, filed on May 31, 2001, now Pat. No. 6,664,569.

(30) **Foreign Application Priority Data**

Jun. 9, 2000 (KR) 2000-31848

(51) **Int. Cl.**
G02F 1/136 (2006.01)
G02F 1/1343 (2006.01)

(52) **U.S. Cl.** 349/46; 349/139

(58) **Field of Classification Search** 349/46,
349/139, 43; 257/59, 72

See application file for complete search history.

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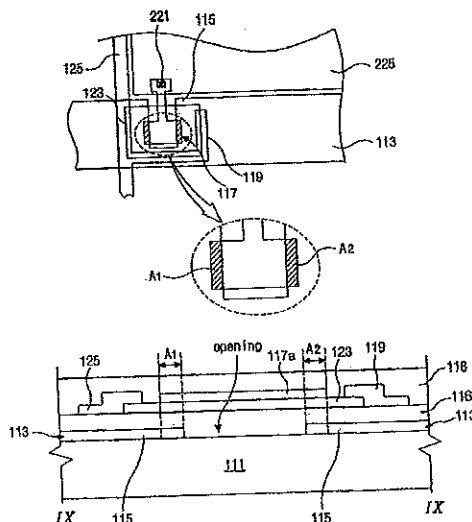
Primary Examiner—Toan Ton

(74) *Attorney, Agent, or Firm*—McKenna Long & Aldridge LLP

ABSTRACT

(57) An array substrate for use in a liquid crystal display device includes a thin film transistor as a switching element, having a gate electrode, a source electrode and a drain electrode, wherein the gate electrode is a portion of a gate line near the crossing of the gate and data lines, and has an inverted "T"-shaped opening or a rectangularly-shaped opening. The drain electrode is shaped like the inverted "T"-shape and corresponds to the opening of the gate electrode. The source electrode surrounds the drain electrode along the steps of the semiconductor layer. Accordingly, in the thin film transistor having this structure, the gate electrode is only overlapped by the edges of the drain electrode. And thus, the gate-drain parasitic capacitance is reduced and minimized. Also, variations in the gate-drain parasitic capacitance are prevented. As a result, a high resolution is achieved and the picture quality is improved in the liquid crystal display device.

7 Claims, 8 Drawing Sheets



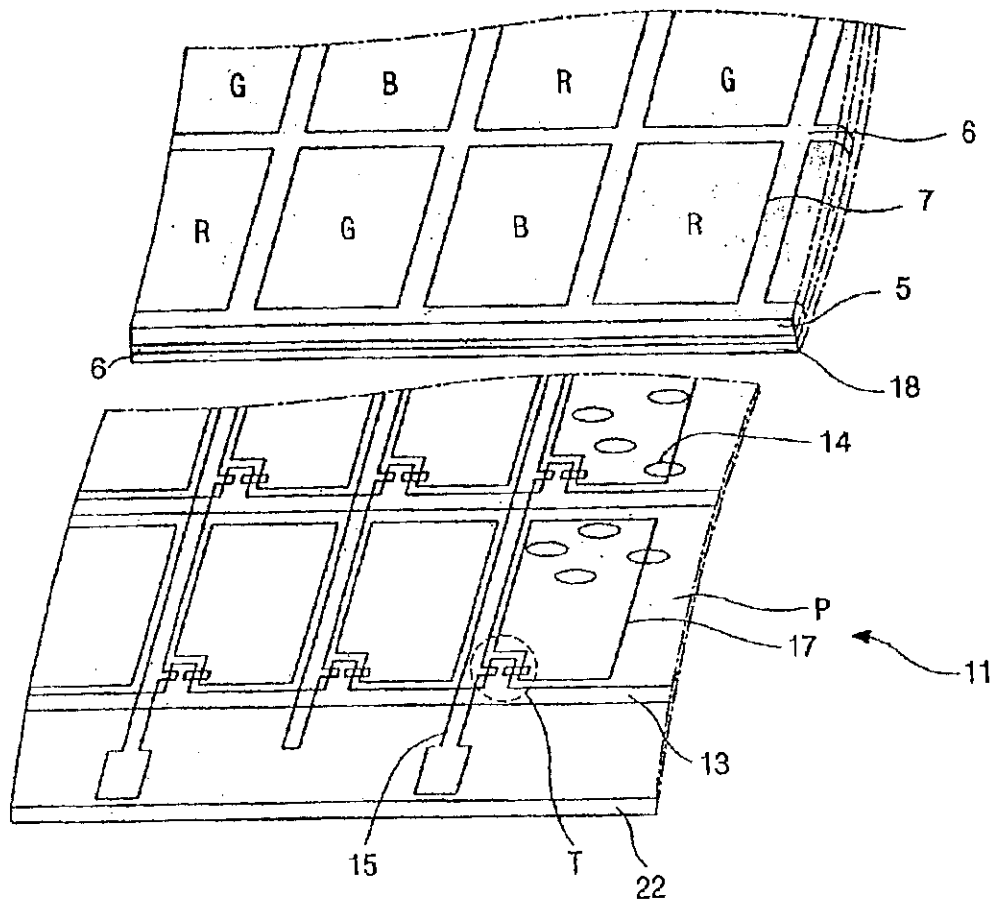
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FIG. 1
(RELATED ART)



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FIG. 2
(RELATED ART)

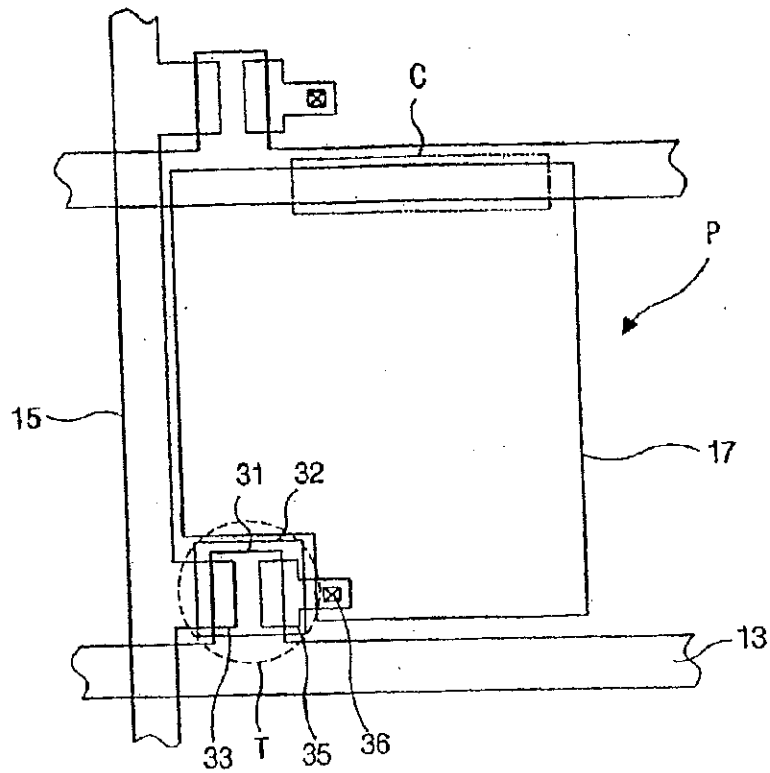
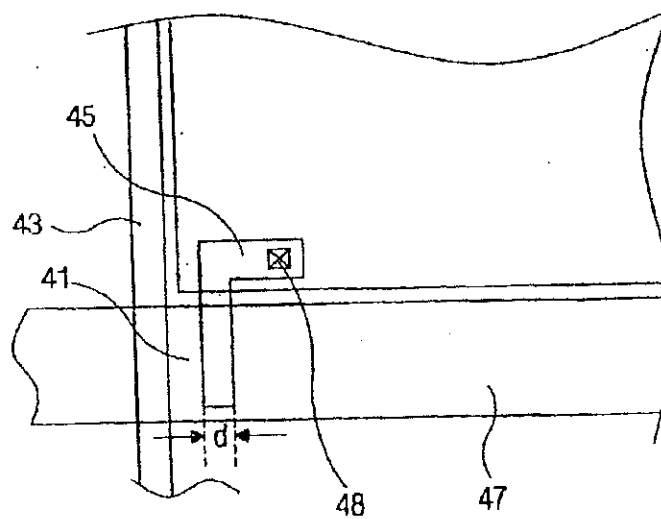


FIG. 3
(RELATED ART)



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FIG. 4
(RELATED ART)

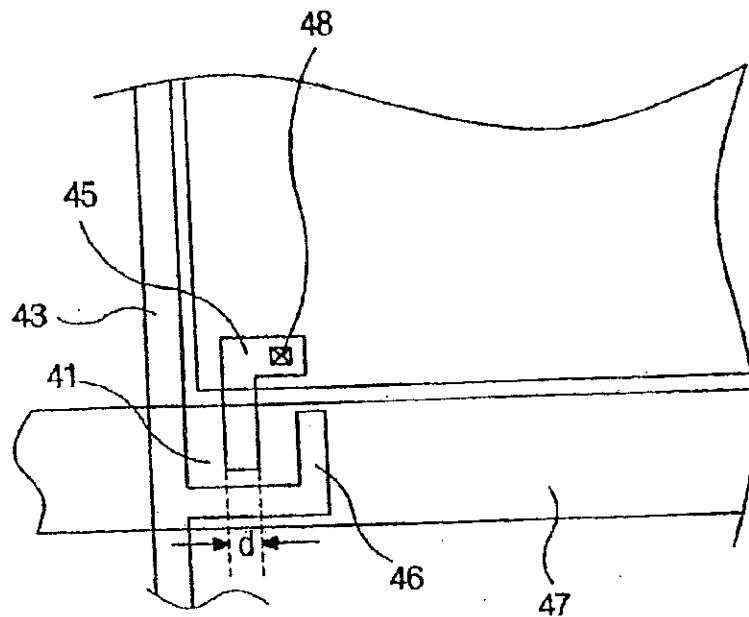
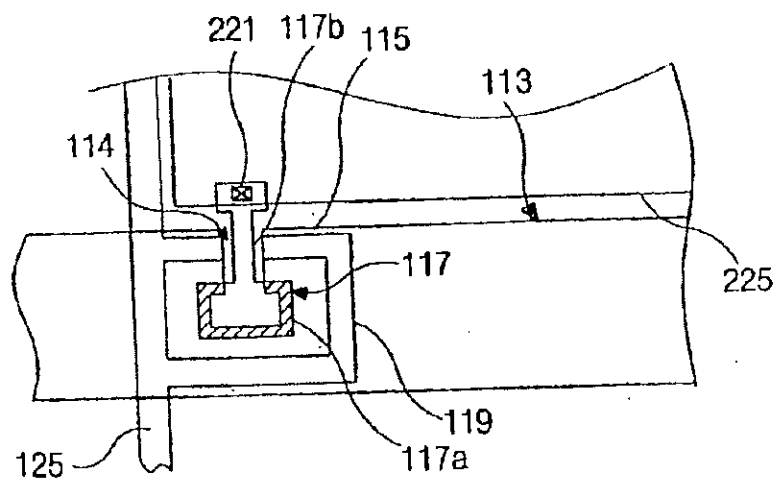


FIG. 5



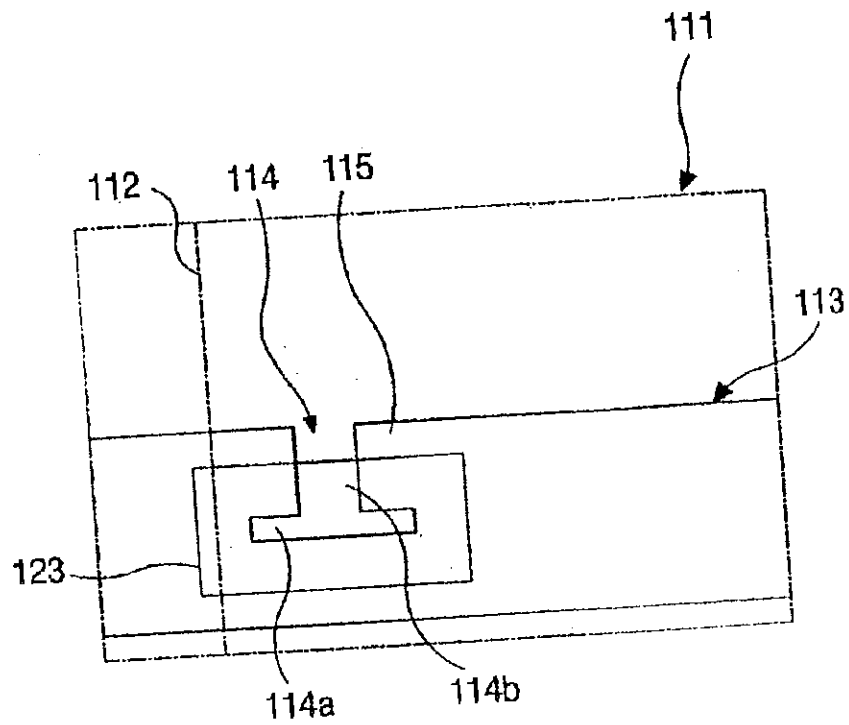
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FIG. 6A



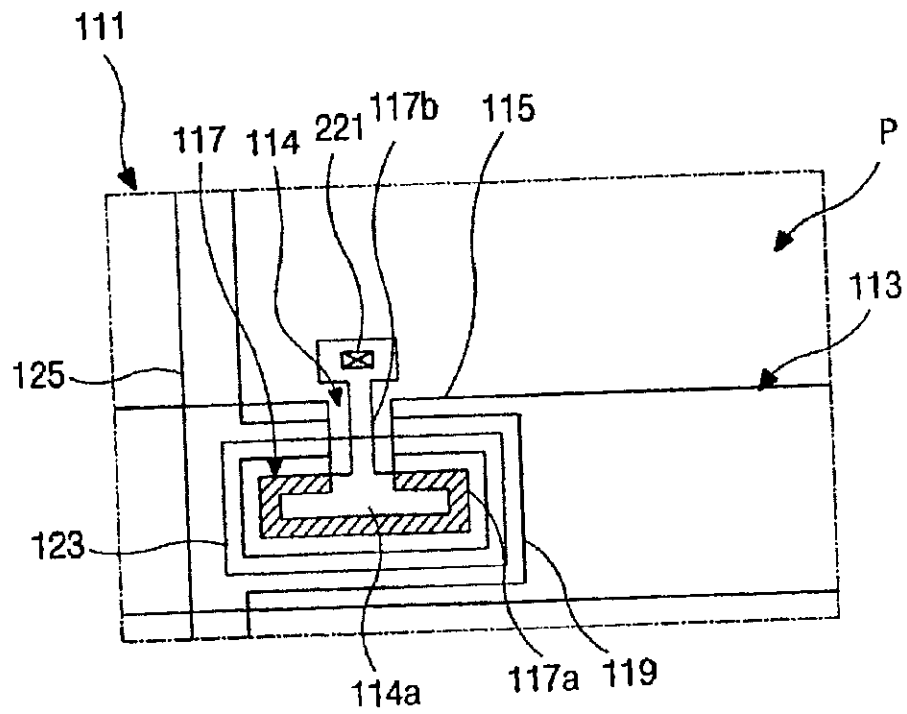
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FIG. 6B



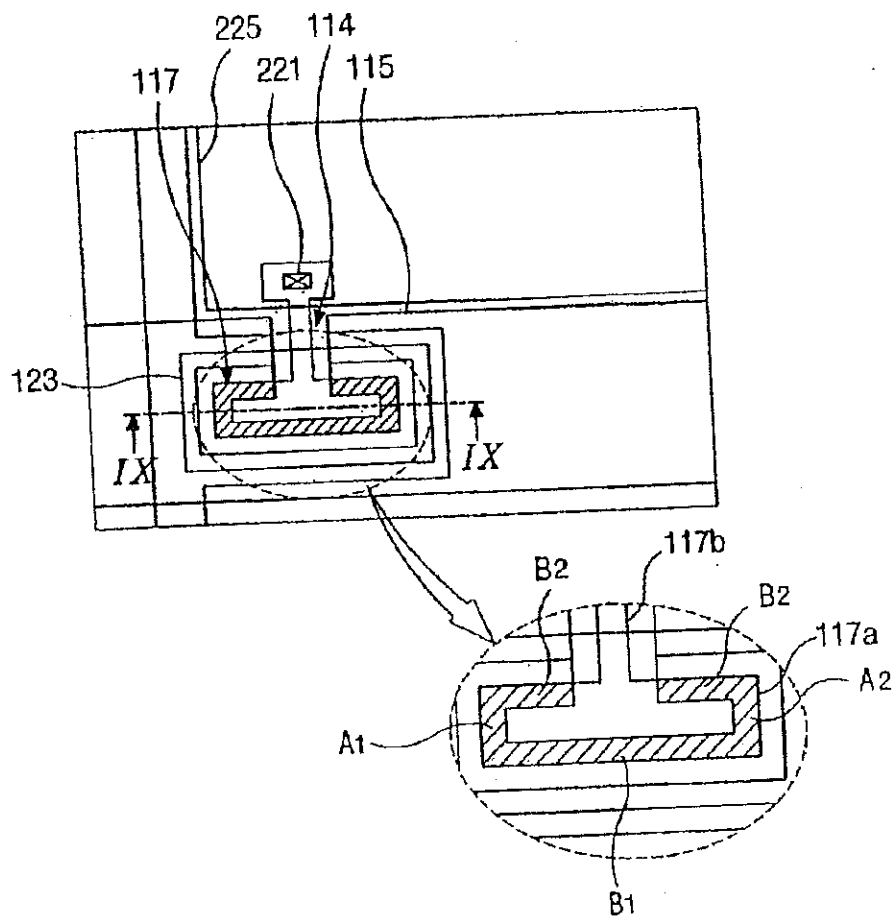
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FIG. 6C



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FIG. 7

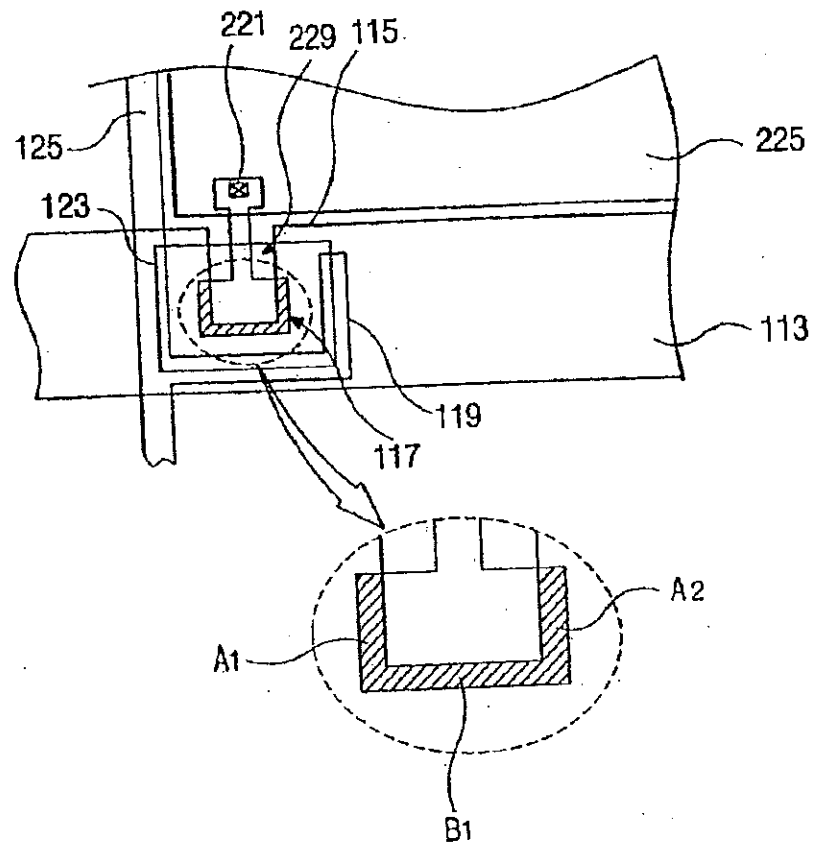


FIG. 8

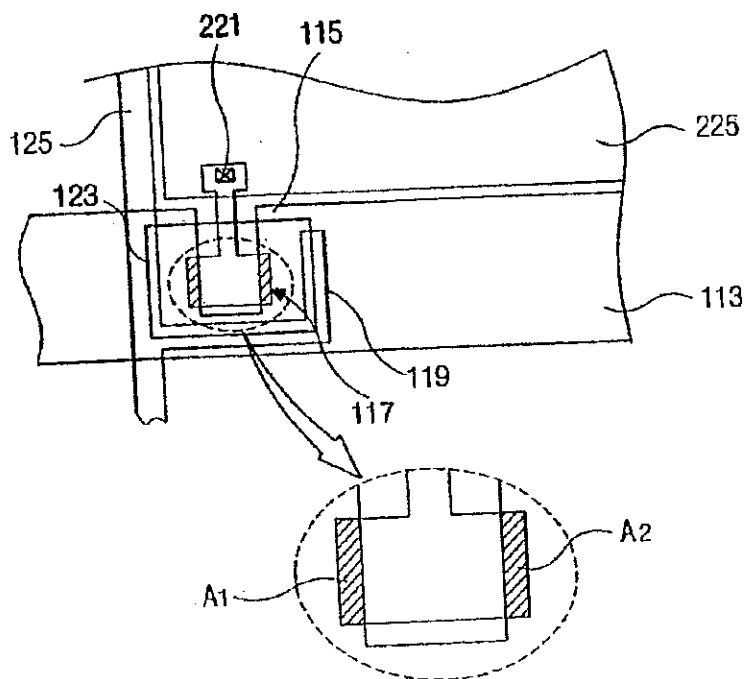
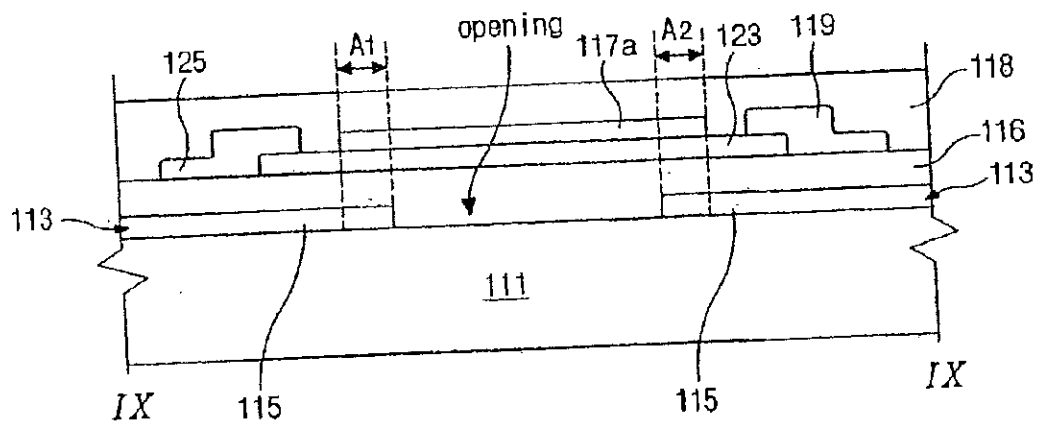


FIG. 9



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LIQUID CRYSTAL DISPLAY DEVICE ARRAY SUBSTRATE AND METHOD OF MANUFACTURING THE SAME

This application is a divisional of prior application Ser. No. 09/867,484, filed May 31, 2001 now U.S. Pat. No. 6,664,569.

This application claims the benefit of Korean Patent Application No. 2000-31848, filed on Jun. 9, 2000, the entirety of which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an array substrate for use in a liquid crystal display (LCD) device, and more particularly, an array substrate having a thin film transistor (TFT) with a reduced parasitic capacitance.

2. Discussion of the Related Art

FIG. 1 shows the configuration of a typical TFT-LCD device. The TFT-LCD device 11 includes upper and lower substrates 5 and 22 with an interposed liquid crystal material 14. The upper and lower substrates 5 and 22 are generally referred to as a color filter substrate and an array substrate, respectively.

On the upper substrate 5, on a surface opposing the lower substrate 22, black matrix 6 and color filter layer 7, including a plurality of red (R), green (G), and blue (B) color filters, are formed in the shape of an array matrix, such that each color filter is surrounded by the black matrix 6. Also, on the upper substrate 5 a common electrode 18 is formed covering the color filter layer 7 and the black matrix 6.

On the lower substrate 22, on a surface opposing the upper substrate 5, a thin film transistor (TFT) "T", as a switching device, is formed in the shape of an array matrix corresponding to the color filter layer 7, and a plurality of crossing gate and data lines 13 and 15 are positioned such that each TFT "T" is located near each crossover point of the gate and data lines 13 and 15. Also, on the lower substrate 22 a plurality of pixel electrodes 17 are formed in an area defined by the gate and data lines 13 and 15. The area defined thereby is called a pixel region "P". The pixel electrode 17 is usually formed from a transparent conductive material having good transmissivity, for example, indium-tin-oxide (ITO) or indium-zinc-oxide (IZO).

The pixel and common electrodes 17 and 18 generate electric fields that control the light passing through the liquid crystal cells provided therebetween. By controlling the electric fields, desired characters or images are displayed.

The operation of the TFT-LCD device having the above-mentioned structure is based on the a principle that the alignment direction of the liquid crystal molecules depends on an applied electric field. Namely, the liquid crystal layer having a spontaneous polarization characteristic is a dielectric anisotropy material. The liquid crystal molecules have dipole moments based on the spontaneous polarization when a voltage is applied. Thus, the alignment direction of the liquid crystal molecules is controlled by applying an electric field to the liquid crystal molecules. When the alignment direction of the liquid crystal molecules is properly adjusted, the liquid crystals are aligned and light is refracted along the alignment direction of the liquid crystal molecules to display image data. The liquid crystal molecules function as an optical modulation element having optical characteristics that vary depending upon the polarity of the applied voltage.

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FIG. 2 is a plan view illustrating one pixel of an array substrate for the liquid crystal display device according to a related art. As shown, the array substrate includes gate line 13 arranged in a transverse direction; data line 15 arranged in a longitudinal direction perpendicular to the gate line 13; and a thin film transistor (TFT) "T" as a switching element formed near the crossing of the gate and data lines 13 and 15. The TFT "T" has a gate electrode 31, a source electrode 33 and a drain electrode 35. The gate electrode 31 is extended from the gate line 13, and the source electrode 33 is extended from the data line 15. The drain electrode 35 is spaced apart from the source electrode 33. The source and drain electrodes 33 and 35 respectively overlap both ends of the gate electrode 31. The TFT "T" also has a semiconductor layer 32 that is made of amorphous silicon (a-Si:H) or poly-silicon.

Moreover, the array substrate further includes a pixel electrode 17 formed on a pixel region "P" that is defined by the gate and data lines 13 and 15. The pixel electrode 17 is electrically connected with the drain electrode 35 through a drain contact hole 36, and is usually made of a transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO). A portion of the pixel electrode 17 overlaps a portion of the gate line 13 such that a storage capacitor "C" is comprised of the pixel electrode 17 and gate line 13 and the interposed dielectric layer (not show).

Still referring to FIG. 2, the gate line 13 supplies scanning signals to the gate electrode 31 of the TFT "T" such that the switching element, i.e., the TFT, turns ON. The scanning signals transmitted to the gate line 13 then control the magnitude of the data signals transmitted from the data line 15 to the pixel electrode 17 via the TFT "T". The data signals of the pixel electrode 17 cause the polarization and re-arrangement of the liquid crystal molecules that are disposed over the pixel electrode 17. When the scanning signals are not supplied to the gate line 13, the TFT "T" is turned OFF. At this time, electric charges stored in the pixel are discharged through the TFT "T" and through the liquid crystals. In this discharge phenomenon, if the off resistance is larger or if the pixel area is smaller for improving the resolution, the electric charges stored in the pixel are more rapidly discharged.

In order to solve these problems, the storage capacitor "C" has a parallel connection with the pixel electrode 17 and compensates for electric discharges. Thus, the data signal is maintained in the pixel. At this time, the data signal, however, is affected by source-gate or drain-gate parasitic capacitance. This effect leads to pixel flickering, image retention and nonuniform display.

In general, the parasitic capacitance occurs between the source and gate electrodes 33 and 31 of the TFT "T" or between the drain and gate electrodes 35 and 31 of the TFT "T". The parasitic capacitance between the source and gate electrodes 33 and 31 is referred to as source-gate or gate-source parasitic capacitance (C_{gs} or C_{sg}). The parasitic capacitance between the drain and gate electrodes 35 and 31 is referred to as drain-gate or gate-drain parasitic capacitance (C_{dg} or C_{gd}). When the semiconductor layer 32 is fully saturated by the electric charges, the gate-drain parasitic capacitance C_{gd} is increased due to the fact that the electric charges stored in the pixel electrode 17 are transmitted to the drain electrode 35. Again, this parasitic capacitance causes pixel flickering, the image retention, and gray scale nonuniformity. Thus, it is essentially required to decrease the gate-drain parasitic capacitance C_{gd} .

Still referring to FIG. 2, the gate electrode 31 is protruded from the gate line 13 over the pixel region "P" near the

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crossing of the gate and data lines 13 and 15. The source and drain electrodes 33 and 35 overlap both ends of the gate electrode 31. In this structure shown in FIG. 2, the gate-drain parasitic capacitance C_{gd} is defined by an area in which the drain electrode 35 overlaps the gate electrode 31. Moreover, misalignment often occurs between the gate and drain electrodes 31 and 35 when forming the co-planar source and drain electrodes 33 and 35 over both ends of the gate electrode 31 using a pattern process. Thus, the gate-drain parasitic capacitance C_{gd} varies owing to this misalignment between the gate and drain electrodes 31 and 35. For example, if the width and length of the drain electrode 35 are respectively 30 μm and 5 μm , the ratio of the width and the length is 30 to 5. In this case, the overlapped ratio of the drain electrode 35 is usually determined to be 30 to 4, and thus the overlapped area between the drain and gate electrodes becomes 120 μm^2 (i.e., 30 $\mu\text{m} \times 4 \mu\text{m}$). However, if the drain electrode 35 horizontally further overlaps by 1 μm , the overlapped area between the gate and drain electrodes 31 and 35 is 150 μm^2 (i.e., 30 $\mu\text{m} \times 5 \mu\text{m}$). Further, if the drain electrode 35 horizontally less overlaps by 1 μm , the overlapped area between the gate and drain electrodes 31 and 35 is 90 μm^2 . These means that a misalignment of 1 μm causes great variations of the gate-drain parasitic capacitance C_{gd} by 25%.

As described above, the parasitic capacitance fluctuates depending on the overlapped area, and the unstable parasitic capacitance affects the data signal transmitted from the data line to the pixel electrode through the TFT. Accordingly, the display characteristics of the liquid crystal display become irregular. As a result, the picture quality is deteriorated by these irregular display characteristics.

FIGS. 3 and 4 are schematic partial plan views illustrating the crossover point of the gate and data lines of an array substrate for the liquid crystal display device according to another related art. As shown, in contrast to the above-mentioned array substrate, a gate electrode 41 is formed in the gate line 47. Namely, a portion of the gate line 47, near the crossing of the gate and data lines 47 and 43, is used as the gate electrode 41. In order to form the TFT, a drain electrode 45 is formed over the gate line 47. Thus, the gate-drain parasitic capacitance C_{gd} is determined by an area of the drain electrode 45.

Referring to FIG. 3, a portion of the data line 43, in which the gate line 47 is overlapped, functions as a source electrode. However, although FIG. 4 is similar to FIG. 3, a source electrode 46 of FIG. 4 is extended from the gate line 43 over the gate line 47. As shown in FIG. 4, the source electrode 46 has a U-shape in order to increase the width of the channel region between the drain electrode 45 and the source electrode 46. Even though the structure of the drain electrode 45 causes parasitic capacitance, as shown in FIGS. 3 and 4, the variation of the parasitic capacitance that is caused by the misalignment is smaller than the above-mentioned TFT depicted in FIG. 2. However, whenever the drain electrode pattern becomes smaller and smaller in order to lower the parasitic capacitance, the process control for forming the drain electrode is difficult and at least an error of about 1 μm surely occurs in the overlapped area. And thus, a critical dimension loss occurs during the patterning process.

In order to overcome the above-mentioned problem, the drain electrode 45 is designed to have a sufficiently large dimension. Thus, the horizontal length "d" is enlarged. At this time, the gate-drain parasitic capacitance C_{gd} however, is also enlarged.

Accordingly, as described before, due to not only the gate-drain parasitic capacitance but also the variation of that

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parasitic capacitance, the pixel flickering and other image deteriorations occur in the liquid crystal display device.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to an array substrate of a liquid crystal display device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

To overcome the problems described above, the present invention provides an array substrate that has a novel structure for decreasing the gate-drain parasitic capacitance.

Another object of the invention is to provide an array substrate that decreases an overlapped area between gate and drain electrodes.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims thereof as well as the appended drawings.

To achieve these and other objects and in accordance with the purpose of the present invention, as embodied and broadly described, an array substrate for use in a liquid crystal display device having a lower gate-drain parasitic capacitance includes a gate line arranged in a horizontal direction on a substrate; a data line arranged in a vertical direction perpendicular to the gate line over the substrate; and a thin film transistor formed near the crossing of the gate and data lines, the thin film transistor comprising a gate electrode that is a portion of the gate line near the crossing, wherein the gate electrode has an open portion in its central portion, a first insulation layer on the gate electrode, a semiconductor layer formed on the first insulation layer and over the gate electrode, a drain electrode formed on the semiconductor layer and over the gate electrode, the drain electrode corresponding to the open portion of the gate electrode, and a source electrode extended from the data line and formed in the same plane as the drain electrode, the source electrode surrounding the drain electrode and the open portion of the gate electrode along the steps of the semiconductor layer.

The array substrate further includes a second insulation layer formed over the thin film transistor, the second insulation layer having a drain contact hole that exposes a portion of the drain electrode; and a pixel electrode formed in a pixel region that is defined by the gate and data lines, the pixel electrode contacting the drain electrode through the drain contact hole.

In one embodiment, the open portion of the gate electrode has an inverted "T"-shape and first and second open portions. The first open portion is formed in a horizontal direction parallel with the gate line and the second open portion is formed in a vertical direction perpendicular to the first open portion. The drain electrode also has an inverted "T"-shape and includes first and second electrode portions. The first electrode portion is arranged in a horizontal direction parallel with the gate line and corresponds to the first open portion of the gate electrode. And the second electrode portion is arranged in a vertical direction perpendicular to the first electrode portion and corresponds to the second open portion.

The open portion of the gate electrode can also be shaped like a rectangle.

Edges of the first electrode portion of the drain electrode overlap the gate electrode. Namely, two or three side edges of the first electrode portion overlap the gate electrode.

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It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWING

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

In the drawings:

FIG. 1 shows the configuration of a typical TFT-LCD device;

FIG. 2 is a plan view illustrating one pixel of an array substrate for the liquid crystal display device according to a related art;

FIGS. 3 and 4 are schematic partial plan views illustrating the crossover point of the gate and data lines of an array substrate for the liquid crystal display device according to related arts;

FIG. 5 is a schematic partial view illustrating the crossover point of the gate and data lines of an array substrate according to a first embodiment;

FIGS. 6A to 6C are plan views illustrating a manufacturing process for the array substrate of FIG. 5;

FIG. 7 is a schematic partial plan view illustrating the crossover point of the gate and data lines of an array substrate according to a second embodiment;

FIG. 8 is a schematic partial plan view illustrating the crossover point of the gate and data lines of an array substrate according to a third embodiment; and

FIG. 9 is a cross-sectional view taken along line IX—IX of FIG. 6C and illustrates layer elements of the thin film transistor according to a principle of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to embodiments of the present invention, which are illustrated in the accompanying drawings.

FIG. 5 is a schematic partial plan view illustrating the crossover point of gate and data lines of an array substrate according to a first embodiment. As shown, the array substrate includes a gate line 113, which is arranged in a horizontal direction, and a data line 125, which is arranged in a vertical direction. The gate line 113 has a portion used for a gate electrode 115 near the crossing of the gate and data lines 113 and 125. In the central portion of the gate line 113 used for gate electrode 115, an inverted "T"-shaped opening 114 is formed. The source electrode 119 is extended from the data line 125, and has a quadrilateral opening in its central portion. Thus, the source electrode 119 surrounds the inverted "T"-shaped opening in the gate line 113. The drain electrode 117 is shaped like the inverted "T"-shape and positioned corresponding to the inverted "T"-shaped opening 114 of the gate electrode 115. Moreover, the drain electrode 117 is divided into a first electrode portion 117a and a second electrode portion 117b. And thus, the source electrode 119 also surrounds the first electrode portion 117a of the drain electrode 117. As shown in FIG. 5, at the end of the second electrode portion 117b of the drain electrode 117, a drain contact hole 221 is formed, and thus a pixel electrode 225 is electrically connected with the drain electrode 117 through this drain contact hole 221.

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Still referring to FIG. 5, in order to decrease an overlapped area between the gate electrode 115 and the drain electrode 117, the portion of the gate electrode 115 under the drain electrode 117 is etched such that the inverted "T"-shaped opening 114 is formed. In other words, the portion of the gate electrode 115 corresponding to the first electrode portion 117a of the drain electrode 117 is etched in a smaller area than the first electrode portion 117a. Thus, edges of the first electrode portion 117a of the drain electrode 117 overlap the gate electrode 115. Moreover, a portion of the gate electrode 115 under the second electrode portion 117b is etched in a wider area than the second electrode portion 117b of the drain electrode 117. Thus, the gate electrode 115 is not overlapped by this second electrode portion 117b.

Accordingly, as described above, since the edges of the first electrode portion 117a of the drain electrode 117 only overlap the gate electrode 115, the gate-drain parasitic capacitance that depends on the overlapped area is minimized.

FIGS. 6A to 6C are plan views illustrating a manufacturing process for the array substrate of FIG. 5, and FIG. 9 is a cross-sectional view taken along line IX—IX of FIG. 6C.

Referring to FIGS. 6A and FIG. 9, a first metal layer is formed on a substrate 111 by depositing a metallic material selected from a group consisting of aluminum (Al), chrome (Cr), molybdenum (Mo), tungsten (W) and the like. After that, the first metal layer is patterned so as to form the gate line 113 in a horizontal direction, and an imaginary line 112 where the data line is formed in a later step is defined. At this time, near the crossover point of the gate line 113 and imaginary line 112, a portion of the gate line 113 is etched so as to form the inverted "T"-shaped opening 114 and the gate electrode 115 is defined there around. The inverted "T"-shaped opening 114 is divided into a first opening portion 114a and a second opening portion 114b. The first opening portion 114a is horizontally disposed in parallel with the gate line 113 in the gate electrode 115, and the second opening portion 114b is vertically elongated from a top edge to a center of the gate line 113 in the gate electrode 115. Thereby, the gate electrode 115 includes the inverted "T"-shaped opening 114 having the first and second opening portion 114a and 114b.

Further, although not depicted in FIG. 6A but shown in FIG. 9, a first insulation layer 116 is formed on the substrate 111 and gate line 113 by depositing an inorganic material, such as silicon nitride (SiN_x) or silicon oxide (SiO_2), or an organic material, such as benzocyclobutene (BCB) or acryl.

Thereafter, an amorphous silicon layer and impurity-included-amorphous silicon layer are formed successively. The amorphous silicon layer and the impurity-included-amorphous silicon layer are patterned into an island-shaped layer so as to form a semiconductor layer 123. As shown in FIG. 6A, the semiconductor layer 123 is located over the inverted "T"-shaped opening 114 of the gate electrode 115 and is larger than the first opening portion 114a.

Referring to FIGS. 6B and 9, a second metal layer is formed on the entire surface of the substrate 111 including the gate line 113, a first insulation layer 116 and the semiconductor layer 123. The second metal layer is the same kind of material as the first metal layer. After that, the second metal layer is patterned so as to form the data line 125 in the area defined by the imaginary line 112 of FIG. 6A. Thus, the data line 125 is perpendicular to the gate line 113 and, with the gate line 113 defines a pixel area "P." During this patterning process, the source electrode 119 extended from the data line 125 is simultaneously formed over the gate

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electrode 115. The shape of the source electrode 119 is a quadrilateral and has a quadrilateral opening therein such that the source electrode 119 surrounds the first opening portion 114a of the inverted "T"-shaped opening 114. Also, the drain electrode 117 is simultaneously formed over the inverted "T"-shaped opening 114 in the same plane as the source electrode 119.

Still referring to FIGS. 6B and 9, the drain electrode 117 is patterned into an inverted "T"-shape and corresponds to the inverted "T"-shaped opening 114 of the gate electrode 115. Again, the drain electrode 117 is divided into the first electrode portion 117a and the second electrode portion 117b. The first electrode portion 117a overlaps the gate electrode 115 such that the edges of the first electrode portion 117a form a "U"-shaped overlapped area (depicted by oblique lines) with the gate electrode 115. The second electrode portion 117b is vertically extended from the first electrode portion 117a over the pixel area "P," and does not overlap the gate electrode 115 due to the fact that the second electrode portion 117b is narrower than the second opening portion 114b of FIG. 6A. Moreover, the drain electrode 117 is spaced apart from the source electrode 119, and the first electrode portion 117a of the drain electrode 117 is surrounded by the source electrode 119 along the steps of the semiconductor layer 123.

Further, although not depicted in FIG. 6B but depicted in FIG. 9, a second insulation layer 118 is formed on the above-mentioned intermediates by depositing an inorganic material, such as silicon nitride (SiN_x) or silicon oxide (SiO_2), or an organic material, such as benzocyclobutene (BCB) or acryl. Next, the second insulation layer (not shown) is patterned in order to form a drain contact hole 221 at the end of the second electrode portion 117b of the drain electrode 117.

Now, referring to FIG. 6C, a transparent conductive material such as indium-tin-oxide (ITO) or indium-zinc-oxide (IZO) is deposited on the above-mentioned second insulation layer. After that, the transparent conductive material is patterned to form a pixel electrode 225 in the pixel region "P" (see FIG. 6B). And thus, the pixel electrode 225 contacts the drain electrode 117 through the drain contact hole 221.

As described hereinbefore, since only the edges of the first electrode portion of the drain electrode overlaps the gate electrode, the gate-drain parasitic capacitance C_{gd} is reduced and minimized due to the smaller overlapped area. Moreover, referring to the enlarged view of the first electrode portion of the drain electrode as shown in FIG. 6C, the compensation for any misalignment will be explained. When forming the drain electrode 117 over the inverted "T"-shaped opening 114 of the gate electrode 115, the drain electrode 117 can be misaligned in a horizontal or vertical direction. If the left portion "A₁" of the overlapped area is decreased due to horizontal misalignment, the right portion "A₂" is increased. In this manner, if the bottom portion "B₁" of the overlapped area is decreased due to vertical misalignment, the top portion "B₂" is increased. Thus, the overlapped area between the drain electrode 117 and the gate electrode 115 is maintained uniformly even though misalignment occurs. Therefore, the variation of the gate-drain parasitic capacitance is reduced and minimized.

FIG. 7 is a schematic partial plan view illustrating the crossover point of the gate and data lines of an array substrate according to a second embodiment. As shown, the second embodiment is similar to the first embodiment depicted in FIG. 5 and the manufacturing process is the same

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as the first embodiment depicted in FIGS. 6A to 6C and in FIG. 9. However, the gate line 113 has a rectangle-shaped opening 229 in a portion for the gate electrode 115.

Referring to FIG. 7, the source electrode 119 is extended from the data line and has a "U"-shape. The drain electrode 117 is formed into an inverted "T"-shape and located over the rectangle-shaped opening 229 of the gate electrode 115. The drain electrode 117 is also surrounded by the source electrode 119 along the steps of the semiconductor layer 123, as in the first embodiment. Moreover, edges of the drain electrode 117 overlap the gate electrode 115, and thus the overlapped area is formed generally with a "U"-shape (depicted by oblique lines). As a result, the gate-drain parasitic capacitance C_{gd} is reduced and minimized as in the first embodiment.

Moreover, referring to the enlarged view of the drain electrode 117 of FIG. 7, any misalignment occurring in the step of forming the drain electrode 117 over the rectangle-shaped opening 229 of the gate electrode 115, the drain electrode 117 can be misaligned in a horizontal or vertical direction. If the left portion "A₁" of the overlapped area is decreased due to horizontal misalignment, the right portion "A₂" is increased. In this manner, if the bottom portion "B₁" of the overlapped area is decreased due to vertical misalignment, the left and right portions "A₁" and "A₂" are increased. Thus, the overlapped area between the drain electrode 117 and the gate electrode 115 is maintained uniformly even though the misalignment occurs. Therefore, the variation of the gate-drain parasitic capacitance is lowered and minimized.

FIG. 8 is a schematic partial view illustrating the crossover point of the gate and data lines of an array substrate according to a third embodiment. As shown, the third embodiment is similar to the second embodiment and the manufacturing process is the same as the second embodiment. However, the overlapped area (depicted by oblique lines) is formed on both end sides of the drain electrode 117.

As shown in FIG. 8, the gate line 113 is arranged in a horizontal direction and the data line 125 is arranged in a vertical direction perpendicular to the gate line 113. The source electrode 119 is extended from the data line 125 and has a "U"-shape. A rectangle-shaped opening is formed in a portion for the gate electrode 115 in the gate line 113. Also, the drain electrode 117 is formed over the rectangle-shaped opening of the gate electrode 115. Although the drain electrode 117 has an inverted "T"-shape, only both end sides of the drain electrode 117 overlap the gate electrode. Thus, the overlapped area (depicted in oblique lines) is reduced and minimized, and the gate-drain parasitic capacitance C_{gd} is also reduced and minimized.

Moreover, referring to the enlarged view of the drain electrode 117 as shown in FIG. 8, any misalignment occurring in the step of forming the drain electrode 117 is compensated. When forming the drain electrode 117 over the rectangle-shaped opening of the gate electrode 115, the drain electrode 117 can be misaligned in a horizontal direction. If the left portion "A₁" of the overlapped area is decreased due to horizontal misalignment, the right portion "A₂" is increased. Thus, the overlapped area between the drain electrode 117 and the gate electrode 115 is maintained uniformly even though misalignment occurs. Therefore, the variation of the gate-drain parasitic capacitance is reduced and minimized.

As described hereinbefore, according to the principles of the present invention, a portion of the gate line is used as the

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gate electrode. And a portion of the gate electrode is patterned so as to form a certain-shaped opening. Accordingly, there is a reduced overlap area between the gate electrode and the drain electrode. As a result, the gate-drain parasitic capacitance is reduced and minimized. Moreover, although misalignment occurs between the drain and gate electrodes, this misalignment is compensated according to the present invention. Thus, the variation of the gate-drain parasitic capacitance is prevented.

Therefore, flickering and the image retention are prevented so that a high resolution is achieved in the liquid crystal display device. And the picture quality is improved in the liquid crystal display device.

It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method of forming a liquid crystal display device, comprising:

forming a gate line on a substrate, the gate line extending along a first direction and having an opening therein;
forming a first insulating layer on the gate line;
forming a semiconductor layer on the first insulating layer over at least a portion of the opening;

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forming a data line on the insulating layer extending along a second direction substantially perpendicular to the first direction, a drain electrode on the semiconductor layer over at least a portion of the opening and, and a source electrode on the semiconductor layer extending from the data line and separated and spaced apart from the drain electrode.

2. The method of claim 1, further comprising forming a second insulation layer over the semiconductor layer and the source and drain electrodes, the second insulation layer having a drain contact hole that exposes a portion of the drain electrode.

3. The method of claim 2, further comprising forming a pixel electrode in a pixel region that is defined by an intersection of the gate and data lines, the pixel electrode contacting the drain electrode through the drain contact hole.

4. The method of claim 1, wherein the opening in the gate line is formed in substantially a "T" shape.

5. The method of claim 1, wherein the source electrode is formed to substantially surround the drain electrode.

6. The method of claim 1, wherein the drain electrode is formed in substantially a "T" shape.

7. The method of claim 1, wherein forming the drain electrode comprises forming a first portion which overlaps the opening and a second portion which overlaps the gate line on at least two opposing sides of the opening.

* * * * *

EXHIBIT 10

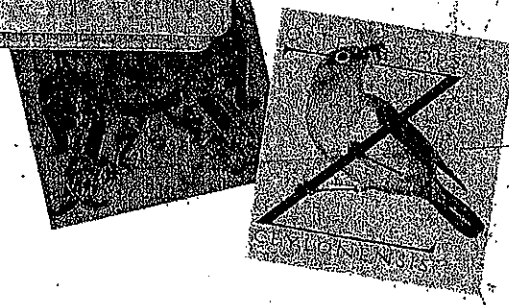
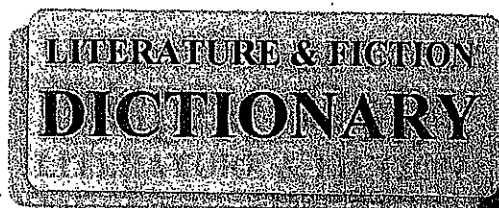
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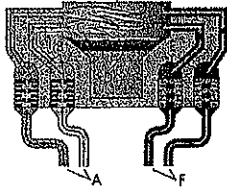
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open-hearth
A. gas and air enter
B. pre-heated chamber
C. molten pig iron
D. hearth
E. heating chamber (cold)
F. gas and air exit

of its endpoints. **b.** Of or being a set such that at least one neighborhood of every point in the set is within the set. **c.** Of or being a set that is the complement of a closed set. **21. Sports a.** Having the forward foot farther from the intended point of impact with the ball than the rear foot: *an open batting stance*. **b.** Held or swung with the top or outer edge of the striking face pointing slightly farther away from the objective than the lower or inner edge: *The club struck the ball with an open face, causing a slice.* **22. *o*-pened, *o*-pening, *o*-pens —*tr.* 1. To release from a closed or fastened position. 2. To remove obstructions from; clear. 3. To make or force an opening in: *open an old wound*. **4a.** To form spaces or gaps between: *soldiers opening ranks*. **b.** To break the continuity of; make a gap in: *open a circuit*. **5a.** To remove the cover, cork, or lid from. **b.** To remove the wrapping from; undo. **6.** To unfold so that the inner parts are displayed; spread out: *open a newspaper*. **7a.** To get (something) going; initiate: *open a campaign*. **b.** To commence the operation of: *open a new business*. **8. Games** To begin (the action in a game of cards) by making the first bid, placing the first bet, or playing the first lead. **9.** To make available for use: *opened the area to commercial development*; *opened the computer file and retrieved some data*. **10.** To make more responsive or understanding. **11.** To reveal the secrets of; bare. **12. Sports** To modify (one's stance), as in baseball or golf, so that it is open. **13. Law** To recall (an order or judgment) for a reexamination of its merits. —*intr.* **1.** To become open: *The door opened slowly*. **2.** To draw apart; separate: *The wound opened under pressure*. **3.** To spread apart; unfold. **4.** To come into view; become revealed: *The plain opened before us*. **5.** To become receptive or understanding. **6a.** To begin; commence: *The meeting opened with a call to order*. **b.** To begin business or operation: *The store opens early on Saturday*. **7.** To be performed, shown, or made available to the public for the first time: *The play opens next week*. **8.** To be priced or listed at a specified amount when trading begins: *Shares opened high and fell sharply*. **9. Games** To make a bid, bet, or lead in starting a game of cards. **10.** To give access: *The room opens onto a terrace*. **24. *o*-pen** **1.** An unobstructed area of land or water. **2.** The outdoors; camping in the open. **3.** An undisguised or unconcealed state: *brought the problem out into the open*. **4.** A tournament or contest in which both professional and amateur players may participate. —*phrasal verb:* **open up** **1.** To spread out; unfold: *A green valley opened up before us*. **2a.** To begin operation: *The new store opens up next month*. **b.** To begin firing: *The artillery opened up at dawn*. **3. Informal** To speak freely and candidly: *At last the frightened witness opened up and told the truth*. **4.** To make an opening in by cutting: *The surgeon opened up the patient's chest*. **5.** To make available or accessible: *open up new markets*. **6. Informal** To accelerate. Used of a motor vehicle. —*Idioms:* **open fire** To begin firing on. **open (one's) eyes** To become aware of the truth of a situation. (Middle English, from Old English. See *upo* in Appendix I.) —*o*-pen·ly *adv.* —*o*-pen·ness *n.***

open admissions *pl.n.* (used with *a sing.* or *pl. verb*) A policy that permits enrollment of a student in a college or university without regard to academic qualifications. Also called *open enrollment*.

open adoption *n.* An adoption arrangement in which contact between the adoptive and biological parents is allowed or maintained.

open-air (*o*'pan-är') *adj.* Outdoor; *an open-air concert*.

open-and-shut (*o*'pan-an-shüt') *adj.* **1.** So obvious as to present no difficulties; easily settled or determined: *an open-and-shut case*. **2.** *New England & Southeastern New York* Alternating between sunshine and clouds; having variable skies.

open chain *n.* An arrangement of atoms that does not form a ring, as in silicon compounds and various carbon compounds, such as aliphatic hydrocarbons.

open city *n.* A city that is declared demilitarized during a war, thus gaining immunity from attack under international law.

open classroom *n.* **1.** A system of elementary education in which instruction and activities are informally structured, flexible, and individualized. **2.** A school or classroom in which this system is practiced.

open door *n.* **1.** Unhindered opportunity; free access. **2.** Admission to all on equal terms. **3.** A policy whereby a nation trades with all other nations on equal terms. —*o*'pen-door' (*o*'pan-dör', -dör') *adj.*

open-end (*o*'pan-änd') *adj.* **1.** Having no definite limit of duration or amount: *an open-end contract*. **2.** Continually issuing new shares or buying back existing shares from shareholders: *an open-end mutual fund*. **3.** Permitting the borrowing of additional funds under existing terms: *an open-end mortgage*.

open-ended (*o*'pan-än-däd') *adj.* **1.** Not restrained by definite limits, restrictions, or structure. **2.** Allowing for or adaptable to change. **3.** Inconclusive or indefinite: *"faintly bemused and uneasily open-ended about the whole horrible business"* (Charles Michener). **4.** Allowing for a spontaneous, unstructured response: *an open-ended question*. —*o*'pen-ended·ly *adv.* —*o*'pen-ended·ness *n.*

open-end investment company *n.* A mutual fund.

open-end wrench *n.* A wrench having fixed, open jaws on one or both ends.

open enrollment *n.* See *open admissions*.

open-er (*o*'pa-när') *n.* **1.** One that opens, especially a device used to cut open cans or pry up bottle caps. **2. Games a.** The player who starts the betting in cards. **b. openers** Cards of sufficient value to enable the holder to open the betting. **3.** The first act in a theatrical variety show. **4. Sports** The first game in a series. —*Idiom:* **for openers** Informal To begin with: *"Out of 34 potential jurors, they knocked 20 off . . . just for openers"* (Joseph DiMona).

open-eyed (*o*'pan-id') *adj.* **1.** Having the eyes wide open, as in surprise. **2.** Watchful and alert.

open-faced (*o*'pan-fäst') *adj.* **1.** Having a face that seems to ex-

hibit honesty and sincerity. **2.** Having a side uncovered: *an open-faced sandwich*.

open-handed (*o*'pan-hän-däd') *adj.* Giving freely; generous. See *synonyms at liberal*. —*o*'pen-handed·ly *adv.* —*o*'pen-handed·ness *n.*

open-heart (*o*'pan-här') *adj.* **1.** Frank. **2.** Kindly. —*o*'pen-heart·ed·ly *adv.* —*o*'pen-heart·ed·ness *n.*

open-hearth (*o*'pan-härth') *n.* **1.** Designating or being a reverberatory furnace used in the production of high-quality steel. **2.** Of or relating to the steel produced in such a furnace.

open-heart surgery (*o*'pan-här't') *n.* Surgery in which the thoracic cavity is opened to expose the heart and the blood is re circulated and oxygenated by a heart-lung machine.

open house *n.* **1.** A social event in which hospitality is extended to all. **2.** An occasion when a school or institution is open for visiting and observation by the public. **3a.** A period of time during which a house or apartment for sale or rent is held open for public viewing. **b.** A house or apartment open for such viewing.

open-ing (*o*'pö-ning') *n.* **1.** The act or an instance of becoming open or being made to open. **2.** An open space serving as a passage or gap. **3.** A breach or aperture. **4.** A clearing in the woods. **5.** The first part or stage, as of a book. **6.** The first performance the opening of a play. **7.** A formal commencement of operation: *attended the opening of the new museum*. **8. Games** A specific pattern or series of beginning moves in certain games, especially chess. **9.** An opportunity affording a chance of success. See *synonyms at opportunity*. **10.** An unfilled job or position; a vacancy.

opening transaction *n.* **1.** The first transaction for a security during a trading day. **2.** An option order that establishes a new investment position or increases the size of an existing investment position.

open interval *n.* A set of numbers consisting of all the numbers between a pair of given numbers but not including the endpoints.

open letter *n.* A published letter on a subject of general interest, addressed to a person but intended for general readership.

open loop *n.* Engineering A control system that does not have a feedback loop and thus is not self-correcting.

open market *n.* A freely competitive market operating without restrictions.

open marriage *n.* A marriage in which the partners agree that each is free to engage in extramarital relationships.

open-mind (*o*'pan-min-däd') *adj.* Having or showing receptiveness to new and different ideas or the opinions of others. See *synonyms at broad-minded*. —*o*'pen-mind·ed·ly *adv.* —*o*'pen-mind·ed·ness *n.*

open-mouthed (*o*'pan-mouthd', -mouth') *adj.* **1.** Having the mouth open. **2.** Gaping in astonishment or wonder. **3.** Loudly insistent. —*o*'pen-mouth·ed·ly *adv.* —*o*'pen-mouth·ed·ness *n.*

open-pollinated (*o*'pan-pöl'-ä-nä'täd') *adj.* Pollinated without human intervention, as by the wind or insects.

open season *n.* **1.** The period during which it is legal to hunt or catch game or fish. **2. Informal** A time of unrestrained harassment, criticism, or attacks: *"By 1950 it was open season on Communists and their fellow travelers"* (Boston).

open secret *n.* Something supposedly secret but in fact generally known.

open sentence *n.* Mathematics An expression that contains at least one unknown quantity and becomes true or false when a test value is substituted for the unknown.

open sesame *n.* A simple, trusty means of attaining a goal. [From the magical formula *Open Sesame* used by Ali Baba in the *Arabian Nights* to open the door of the robbers' cave.]

open shop *n.* A business or factory in which workers are employed without regard to union membership.

open-source (*o*'pan-sör's', -sör's') *adj.* Of or relating to source code that is available to the public: *an open-source operating system*.

open stock *n.* Merchandise kept in stock so as to enable customers to replace or supplement articles, such as dishes, purchased in sets.

open universe *n.* A model of the universe in which there is insufficient matter, and thus insufficient gravitational force, to halt the expansion initiated by the big bang.

open-work (*o*'pan-würk') *n.* Ornamental or structural work, as of embroidery or metal, containing numerous openings, usually in set patterns.

opera (*o*'pär-ä, o'pä'rä) *n.* **1.** A theatrical presentation in which a dramatic performance is set to music. **2.** The score of such a work. **3.** A theater designed primarily for operas. [Italian, work, opera, from Latin, work, service. See *op-* in Appendix I.]

opera (*o*'pär-ä, o'pä'rä) *n.* A plural of *opus*.

operable (*o*'pär-ä-bäl, o'pä'rä-) *adj.* **1.** Being such that use or operation is possible: *an operable machine*. **2.** Possible to put into practice; practicable: *an operable plan*. **3.** Treatable by surgical operation with a reasonable degree of safety and chance of success: *an operable cancer*. —*o*'pär-ä-bil·i·ty *n.* —*o*'pär-ä-bly *adv.*

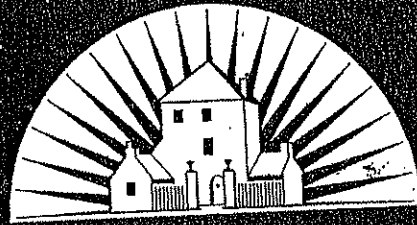
opéra bouffe (*o*'pä'r-ä bööf', o'pä'rä, o-pä-rä bööf') *n.* A comic, often farcical opera. [French, from Italian *opera buffa*. See *OPERA BUFFA*.]

opera buffa (*o*'pä'r-ä bööf'fä, o'pä'rä, o-pä-rä bööf'fä) *n.* An Italian comic opera of the 18th century. [Italian: *opera*, opera + *buffa*, feminine of *buffo*, comic.]

opéra comique (*o*'pä'r-ä kö-mék', o'pä'rä, o-pä-rä kö-mék') *n.* A French comic opera. [French: *opéra*, opera + *comique*, comic.]

opera glass (*o*'pä'r-ä, o'pä'rä) *n.* A pair of small, low-powered bin-

EXHIBIT 11



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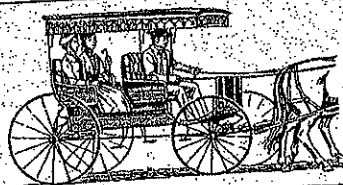


EXHIBIT 12

PAT-NO: JP408171076A

DOCUMENT-IDENTIFIER: JP 08171076 A

TITLE: LIQUID CRYSTAL DISPLAY
ELEMENT AND ITS PRODUCTION

PUBN-DATE: July 2, 1996

INVENTOR-INFORMATION:
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APPL-NO: JP06334977

APPL-DATE: December 19, 1994

INT-CL (IPC): G02F001/13, G02F001/1333 ,

G02F001/1343

ABSTRACT:

PURPOSE: To efficiently and inexpensively produce a liquid crystal display element by making it possible to simultaneously process two kinds of electrode substrates in parallel even in a limited production space, thereby averting excess quality.

CONSTITUTION: A pair of the electrode substrates formed with cut parts varying in sizes in corner parts are sent from a prepn. stage through, for example, a loader stage 15, a washing stage 16 and a resist applying stage 17 to a discriminating stage 18. The respective electrode substrates are discriminated in accordance with the respective cut parts in this discriminating stage 18. The discriminated electrode substrates are respectively subjected to parallel treatments in exposing stages 19, 20 of respectively separate lines. The respective electrode substrates fed in the separate lines are collected to one line and are subjected to the canon processing in a developing stage 21. There is no need for using two lines of the production lines to be exclusively used for respective production of the respective electrode substrates like

heretofore or using one production line by changing over the line at every specified time is eliminated the simultaneous and parallel processing of two kinds of the electrode substrates in the limited production space is possible.

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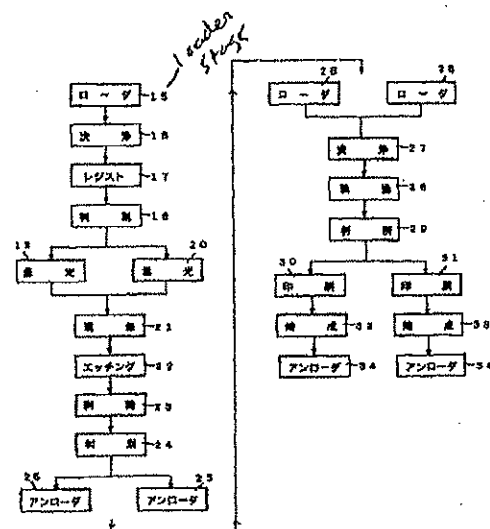
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(54) 【発明の名称】 液晶表示素子およびその製造方法

(57) 【要約】

【目的】 限られた製造スペースでも2種類の電極基板を同時に並列処理でき、過剰品質を回避して液晶表示素子を効率良く安価に生産する。

【構成】 コーナ部分に大きさの異なるカット部が形成された一対の電極基板が準備工程から例えばローグ工程15、洗浄工程16、およびレジスト塗布工程17を経て判別工程18に送り込まれると、この判別工程18で各電極基板それぞれを各カット部に基づいて判別し、判別された各電極基板それぞれを別々のラインの露光工程19、20で並列処理し、別々のラインで送られた各電極基板を現像工程21で1本のラインにまとめて共通の処理をする。したがって、電極基板を2種類にしても、従来のように各電極基板をそれぞれ製造する2本の専用製造ラインを用いたり、1本の製造ラインを一定時間ごとに切り換えて使用したりする必要がなく、限られた製造スペースでも2種類の電極基板を同時に並列処理できる。



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【特許請求の範囲】

【請求項1】 対向面にそれぞれ電極およびこの電極を覆う配向膜が形成された一対の電極基板間に液晶を封入した液晶表示素子において、

前記一対の電極基板にそれぞれを互いに判別可能にする判別情報供給手段を設けたことを特徴とする液晶表示素子。

【請求項2】 前記判別情報供給手段は、前記一対の電極基板それぞれの形状の差であることを特徴とする請求項1記載の液晶表示素子。

【請求項3】 前記判別情報供給手段は、前記一対の電極基板それぞれの厚さの差であることを特徴とする請求項1記載の液晶表示素子。

【請求項4】 前記判別情報供給手段は、前記一対の電極基板それぞれの材質の差であることを特徴とする請求項1記載の液晶表示素子。

【請求項5】 前記判別情報供給手段は、前記一対の電極基板の前記電極それぞれの膜厚の差であることを特徴とする請求項1記載の液晶表示素子。

【請求項6】 前記判別情報供給手段は、前記一対の電極基板の前記電極それぞれの材質の差であることを特徴とする請求項1記載の液晶表示素子。

【請求項7】 前記判別情報供給手段は、前記電極基板と前記電極とを合わせた全体のそれぞれの厚さの差であることを特徴とする請求項1記載の液晶表示素子。

【請求項8】 前記判別情報供給手段は、前記一対の電極基板に形成された識別マークであることを特徴とする請求項1記載の液晶表示素子。

【請求項9】 対向面に電極膜が形成され、かつ両者を判別可能にする判別情報供給手段を備えた一対の電極基板を準備する準備工程と、
前記判別情報供給手段に基づいて前記一対の電極基板のそれぞれを判別する判別工程と、
前記判別工程で判別された前記各電極基板をそれぞれ別のラインで搬送しながら並列処理する並列処理工程と、
前記並列処理工程の別々のラインで搬送されてきた前記各電極基板を1本のラインにまとめて順次搬送しながら共通の処理をする共通処理工程と、
からなることを特徴とする液晶表示素子の製造方法。

【請求項10】 前記判別工程、前記並列処理工程、および前記共通処理工程は、繰り返し行なわれることを特徴とする請求項9記載の液晶表示素子の製造方法。

【請求項11】 前記並列処理工程は、前記電極膜を所定形状の電極にパターンニングするためのフォトリソの露光工程であることを特徴とする請求項9または10記載の液晶表示素子の製造方法。

【請求項12】 前記並列処理工程は、前記電極膜が所定形状にパターンニングされた電極を覆う配向膜を形成する配向膜形成工程であることを特徴とする請求項9または10記載の液晶表示素子の製造方法。

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【発明の詳細な説明】

【0001】

【産業上の利用分野】この発明は、液晶表示素子およびその製造方法に関する。

【0002】

【従来の技術】一般に、液晶表示素子は、一対の電極基板の対向面にそれぞれ透明導電材料からなる電極およびこの電極を覆う配向膜が形成され、これら一対の電極基板間に液晶がシール材によって封入された構造になっている。この場合、一方の電極基板には電極として信号電極が形成され、他方の電極基板には電極としてコモン電極が形成されている。このような液晶表示素子では、通常、部品点数や製造工程などの煩雑さを避けるために、一対の電極基板および各電極がその材料や膜厚などを同じにした同一仕様になっている。

【0003】

【発明が解決しようとする課題】しかしながら、このような液晶表示素子では、一般に、信号電極はコモン電極よりも長さが短くコモン電極よりも電気抵抗が高くては良いため、コモン電極の膜厚よりも薄く形成することができるが、一対の電極基板および各電極を同一仕様とするためには、信号電極もコモン電極と同じ厚さに形成されることになり、一方が他方に対して過剰品質になり、この分コスト高になるという問題があった。このようなことから、一対の電極基板を2種類にすることが検討されている。このように一対の電極基板を2種類にした場合には、以下のような製造方法を採用する必要がある。すなわち、各電極基板をそれぞれ製造するための2本の専用の製造ラインを用いる方法、あるいは1本の製造ラインを一定時間ごとに切り換えて使用する方法などがある。しかしながら、前者の製造方法では、2本の専用の製造ラインを設置しなければならないため、広い製造スペースが必要で、設備費用がかさみ、製造コストが高くなるという問題が生じる。また、後者の製造方法では、1本の製造ラインを一定時間ごとに切り換えて使用するため、生産効率が悪く、生産能力が低下するという問題が生じる。

【0004】この発明の第1の目的は、一対の電極基板をそれぞれ別の種類にして過剰品質を防ぎ、低価格化を図ることのできる液晶表示素子を提供することである。また、この発明の第2の目的は、限られた製造スペースでも2種類の電極基板を同時に並列処理でき、効率良く生産することのできる液晶表示素子の製造方法を提供することである。

【0005】

【課題を解決するための手段】請求項1記載の発明は、上記第1の目的を達成するため、対向面にそれぞれ電極およびこの電極を覆う配向膜が形成された一対の電極基板間に液晶を封入した液晶表示素子において、一対の電極基板にそれぞれを互いに判別可能にする判別情報供給

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手段を設けたことを特徴とするものである。この場合、請求項1～8に記載の如く、判別情報供給手段は、一対の電極基板それぞれの形状の差、一対の電極基板それぞれの厚さの差、一対の電極基板それぞれの材質の差、一対の電極基板の電極それぞれの膜厚の差、一対の電極基板の電極それぞれの材質の差、電極基板と電極とを合わせた全体のそれぞれの厚さの差、一対の電極基板にそれぞれ形成された識別マークなどのいずれかであることが望ましい。

【0006】また、請求項9記載の発明は、上記第2の目的を達成するため、対向面に電極膜が形成され、かつ両者を判別可能にする判別情報供給手段を備えた一対の電極基板を準備する準備工程と、判別情報供給手段に基づいて一対の電極基板のそれぞれを判別する判別工程と、この判別工程で判別された各電極基板をそれぞれ別のラインで搬送しながら並列処理する並列処理工程と、この並列処理工程の別々のラインで搬送されてきた各電極基板を1本のラインにまとめて順次搬送しながら共通の処理をする共通処理工程とからなることを特徴とするものである。この場合、請求項10に記載の如く、判別工程、並列処理工程、および共通処理工程は、繰り返し行なわれることが望ましい。また、請求項11に記載の如く、並列処理工程は電極膜を所定形状の電極にパターンニングするためのフォトリソの露光工程であり、また請求項12に記載の如く、電極膜が所定形状にパターンニングされた電極を覆う配向膜を形成する配向膜形成工程であることが望ましい。

【0007】

【作用】請求項9記載の発明によれば、判別情報供給手段を備えた一対の電極基板が準備工程から判別工程に送り込まれると、この判別工程で一対の電極基板のそれぞれを判別情報供給手段に基づいて判別し、判別された各電極基板それぞれを並列処理工程の別々のラインで搬送しながら並列処理し、別々のラインで搬送されてきた前記各電極基板を共通処理工程で1本のラインにまとめて順次搬送しながら共通の処理をするので、電極基板を2種類にしても、従来のように各電極基板をそれぞれ製造するための2本の専用の製造ラインを用いたり、あるいは1本の製造ラインを一定時間ごとに切り換えて使用したりする必要がなく、限られた製造スペースでも2種類の電極基板を同時に並列処理でき、効率良く生産することができる。

【0008】また、請求項1記載の発明によれば、一対の電極基板のそれぞれを判別可能にする判別情報供給手段を備えているので、電極基板を2種類にしても、請求項9に記載の如く判別情報供給手段に基づいて2種類の電極基板を判別して別々のラインで同時に並列処理でき、効率良く生産することができ、したがって一対の電極基板それぞれの材質や厚さ、あるいは各電極の材質や厚さなどを種類ごとに変えることにより、電極を有する

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一対の電極基板をそれぞれ別の種類にして過剰品質を防ぐことができ、これにより製品の単価を下げることができ、製品の低価格化を図ることができる。

【0009】

【実施例】以下、図1～図3を参照して、この発明の液晶表示素子およびその製造方法の一実施例について説明する。図1はこの発明の液晶表示素子を示す断面図である。この液晶表示素子は、ガラスや合成樹脂などからなる一対の電極基板1、2の対向面に電極3、4および各電極3、4をそれぞれ覆う配向膜5、6が形成され、これら一対の電極基板1、2の対向する配向膜5、6間に液晶7がシール材8により封入された構造になっている。

【0010】電極3、4はITOなどの透明な導電材料からなり、一方の電極基板1の電極3は左右方向に長い帯状のコモン電極であり、他方の電極基板2の電極4は紙面の表裏方向に長い帯状の信号電極であり、各電極3、4は互いに直交した状態で対向している。また、信号電極4は、コモン電極3よりも長さが短くなっており、このためコモン電極3のように電気抵抗を低く抑える必要がないので、コモン電極4よりも膜厚が薄く形成されている。したがって、一対の電極基板1、2は、同一仕様でなく、それぞれ仕様が異なる。

【0011】また、一方の電極基板1のコーナ部分には、判別情報供給手段として、例えば図2(a)に示すように、2mmの隅切りカット部10が形成されている。このカット部10に対応する他方の基板2のコーナ部分には、判別情報供給手段として、例えば図2(b)に示すように、4mmの隅切りカット部11が形成されている。これにより、一対の電極基板1、2は、カット部10、11の大きさが異なることにより、それぞれ異なる形状に形成されていることになる。なお、カット部10、11の大きさは2mm単位で形成されているが、その理由は現状の接触式センサによる検出が2mmの外形差を有していないと不可能になるからである。

【0012】次に、図3を参照して、この液晶表示素子の製造方法について説明する。まず、仕様の異なる2種類の電極基板1、2を準備する。すなわち、準備された電極基板1、2のうち、一方の電極基板1には予めコモン電極3用の電極膜が所定の膜厚で形成されており、コーナ部分には2mmのカット部10が形成されている。また、他方の電極基板2には予め信号電極4用の電極膜がコモン電極3用の電極膜よりも薄い膜厚で形成されており、コーナ部分には4mmのカット部11が形成されている。

【0013】そして、各電極基板1、2は、ロード工程15から順次洗浄工程16に送り込まれて洗浄され、レジスト工程17に搬送され、このレジスト工程17で各電極基板1、2の電極膜上にフォトリソが塗布される。フォトリソが塗布された各電極基板1、2は、

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判別工程18で各種類ごとに判別されて振り分けられる。すなわち、この判別工程18では、各電極基板1、2のそれぞれのカット部10、11が接触式センサなどで検知されることにより、各電極基板1、2の種類が判別される。そして、各種類ごとに判別されて振り分けられた各電極基板1、2は、それぞれ別のラインの露光工程（並列処理工程）19、20に搬送される。各露光工程19、20では、各ラインごとに共通電極3および信号電極4の各電極パターンに応じたそれぞれのマスクを用いてフォトリソを露光する。また、この露光工程19、20では、各種類の電極基板1、2をそれぞれ同時に並列処理する。

【0014】この後、露光工程19、20の別々のラインで搬送された各電極基板1、2は、それぞれ1本のラインにまとめられ、共通処理工程の1つである現像工程21に順次送り込まれ、この現像工程21で各電極基板1、2のフォトリソがそれぞれ現像された上、エッチング工程22に送り込まれる。このエッチング工程22では、それぞれのフォトリソをマスクとして各電極膜がエッチングされ、これにより各電極3、4がそれぞれ形成される。すなわち、一方の電極基板1には共通電極3が、他方の電極基板2には信号電極4がそれぞれ適切な膜厚で形成される。この後、各電極基板1、2は、剥離工程23に順次送り込まれ、この剥離工程23で各フォトリソがそれぞれ剥離された上、次の判別工程24に送り込まれる。この判別工程24では、各電極基板1、2が再び上述と同様に各種類ごとに判別されて振り分けられ、それぞれ別のラインのアンロード工程25に送られる。これにより、各電極3、4の形成工程が終了する。

【0015】次に、アンロード工程25から各電極基板1、2がそれぞれ各ロード工程26に進み、各ロード工程26から各電極基板1、2が再び1本のラインにまとめられ、共通処理工程の1つである洗浄工程27に各電極基板1、2が順次送り込まれてそれぞれ洗浄された上、次の乾燥工程28に送り込まれて順次乾燥される。乾燥された各電極基板1、2は、再び判別工程29で上述と同様に各種類ごとに判別されて振り分けられ、それぞれ並列処理工程の一部である別ラインの各印刷工程30、31に搬送され、各電極基板1、2の電極3、4に応じて配向膜が印刷される。そして、配向膜が印刷された各電極基板1、2は、それぞれ別のラインの焼成工程32、33に送られて各配向膜がそれぞれ焼成され、それぞれ別のラインのアンロード工程34に送られる。これにより、各電極基板1、2に配向膜を形成する配向膜形成工程が終了する。この配向膜形成工程は、一對の電極基板1、2に施す処理は同じであるが、処理に要する時間が長いので、並列処理することにより全体の処理時間の低減に大きく寄与する。

【0016】なお、この後は、図示しないが、一對の電

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極基板1、2の一方の周縁部分にシール材8を印刷し、このシール材8を介して一對の電極基板1、2を張り合わせ、これら一對の電極基板1、2およびシール材8で囲われた領域内にシール材8の注入口から液晶7を注入した上、この注入口を封止することにより、液晶表示素子が完成する。

【0017】このように、この液晶表示素子の製造方法では、一對の電極基板1、2の各コーナ部分に形成された大きさの異なるカット部10、11を判別工程18、24、29で接触式センサなどにより判別し、各電極基板1、2それぞれを並列処理工程である露光工程19、20またはアンロード工程25もしくは印刷工程30、31および焼成工程32、33などのそれぞれ別のラインに振り分けて搬送しながら並列処理し、別々のラインで搬送されてきた各電極基板1、2を共通処理工程である現像工程21、エッチング工程22および剥離工程23、または洗浄工程27および乾燥工程28などのそれぞれ1本のラインにまとめて順次搬送しながら共通の処理をするので、電極基板1、2を2種類にしても、従来のように各電極基板1、2をそれぞれ製造するための2本の専用の製造ラインを用いたり、あるいは1本の製造ラインを一定時間ごとに切り換えて使用したりする必要がなく、限られた製造スペースでも2種類の電極基板1、2を適宜並列に搬送して同時に所要の処理をすることができ、液晶表示素子を効率良く生産することができる。

【0018】また、この液晶表示素子では、一對の電極基板1、2の各コーナ部分にそれぞれ異なる大きさのカット部10、11を形成することにより、一對の電極基板1、2の形状を異ならせて各電極基板1、2をそれぞれ互いに判別可能にしたので、一對の基板1、2自体の厚さや材質および各電極3、4の膜厚や材質をそれぞれの電極基板に適したものとすることにより、基板や電極の過剰品質を防ぐことができ、これにより製品の単価を下げることができ、製品の低価格化を図ることができる。

【0019】なお、上記実施例では、一對の電極基板1、2のそれぞれに設ける各電極3、4の膜厚をそれぞれの電極基板に適する固有の厚さにした場合について述べたが、これに限らず、例えば各電極3、4の材質として高価なITOと安価なSnO₂を電極基板1、2ごとに使い分けても良く、また電極基板1、2自体の厚さを種類ごとに変えても良く、また電極基板1、2としてガラス基板とプラスチック基板、または板状のプラスチック基板とシート状のフィルム基板などのように組み合わせを異ならせても良く、さらにこれらすべての項目をそれぞれ電極基板に適したものにして組み合わせても良い。このようにすれば、製品の単価をより一層下げることができ、極めて低コストの製品を得ることができる。

【0020】また、上記実施例では、カット部10、1

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1を接触式センサで検知する場合について述べて、これに限らず、例えば反射率、透過率、屈折率などを測定する光学式、あるいは超音波式などの非接触式センサなどで検知するようにしても良い。

【0021】また、上記実施例では、各電極基板1、2の1つのコーナ部分にそれぞれ大きさの異なるカット部10、11を形成して各電極基板1、2の形状を異ならせたが、これに限らず、例えば一方の基板のみにカット部を形成するだけでも良く、あるいは同じ大きさのカット部を各電極基板1、2の異なる位置に形成しても良く、またカット部の数を各電極基板1、2で異なる数で形成しても良く、さらにこれらを組み合わせても良い。

【0022】さらに、上記実施例では、判別情報供給手段として、一対の電極基板1、2にカット部10、11を形成して各電極基板1、2の形状を異ならせたが、これに限らず、例えば一対の電極基板1、2の各電極3、4の膜厚を異ならせたものでも良く、また一対の電極基板1、2の各電極3、4をITOやSnO₂などのような異なる材質で形成したものでも良い。この場合には判別対象部材の反射率、透過率、屈折率などを光学的に測定し、材質の差を判別すれば良い。また、これに限らず、一対の電極基板1、2の厚さを異ならせたものでも良く、また一対の電極基板1、2としてガラス基板とプラスチック基板、または板状のプラスチック基板とシート状のフィルム基板などを用い、一対の電極基板1、2の材質をそれぞれ異ならせたものでも良い。さらには、一対の電極基板1、2にそれぞれITOなどの電極膜によって設けられた識別マークで判別するようにしても良い。この場合には検査カメラなどで識別マークを読み取って各電極基板1、2の種類を判別すれば良い。

【0023】

【発明の効果】以上説明したように、請求項9記載の液晶表示素子の製造方法によれば、判別情報供給手段を備えた一対の電極基板が準備工程から判別工程に送り込まれると、この判別工程で一対の電極基板のそれぞれを判別情報供給手段に基づいて判別し、判別された各電極基板それぞれを並列処理工程の別々のラインで搬送しながら並列処理し、別々のラインで搬送されてきた各電極基板を共通処理工程で1本のラインにまとめて順次搬送しながら共通の処理をするので、電極基板を2種類にしても、従来のように各電極基板をそれぞれ製造するための

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2本の専用の製造ラインを用いたり、あるいは1本の製造ラインを一定時間ごとに切り換えて使用したりする必要がなく、限られた製造スペースでも2種類の電極基板を同時に並列処理でき、液晶表示素子を効率良く生産することができる。また、請求項1記載の液晶表示素子によれば、一対の電極基板のそれぞれを判別可能にする判別情報供給手段を備えているので、電極基板を2種類にしても、請求項9に記載の如く判別情報供給手段に基づいて2種類の電極基板を判別して別々のラインで同時に並列処理でき、液晶表示素子を効率良く生産することができ、したがって一対の基板それぞれの材質や厚さ、あるいは各電極の材質や厚さなどをそれぞれの電極基板に適したものとするにより、基板や電極などの構成部材の過剰品質を防ぐことができ、これにより製品の単価を下げることができ、製品の低価格化を図ることができる。

【図面の簡単な説明】

【図1】この発明の液晶表示素子の1例を示す要部断面図。

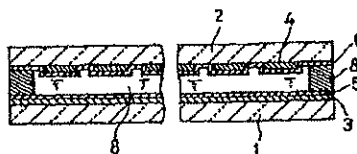
【図2】各電極基板の形状の相違を示し、(a)はコモン電極側の電極基板の平面図、(b)は信号電極側の電極基板の平面図。

【図3】液晶表示素子の製造方法のフローを示す工程図。

【符号の説明】

- 1、2 電極基板
- 3、4 電極
- 5、6 配向膜
- 7 液晶
- 8 シール材
- 10、11 カット部
- 18、24、29 判別工程
- 19、20 露光工程
- 21 現像工程
- 22 エッチング工程
- 23 剥離工程
- 30、31 印刷工程
- 32、33 焼成工程
- 27 洗浄工程
- 28 乾燥工程

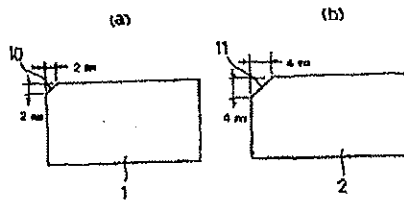
【図1】



(6)

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【図2】



【図3】

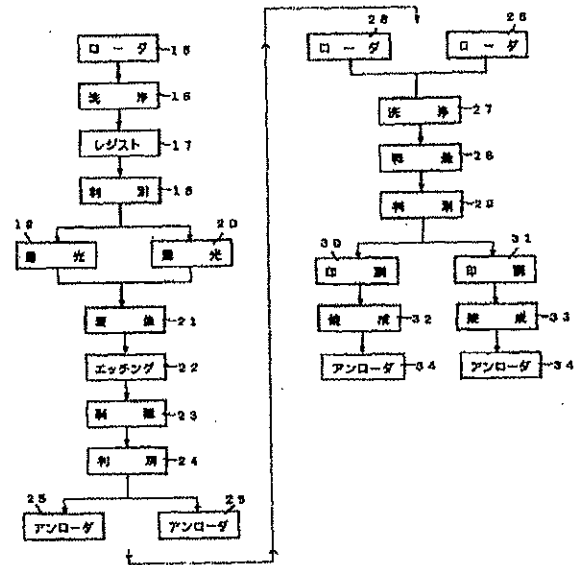


EXHIBIT 13

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salt pan

salt pater

1201

same

before a vowel) ▶ comb. form relating to
salty.
[sɒlˈgætm̩] ▶ n. surgical unblocking of

of Latin American dance music incorp-
rock. ▶ a dance performed to this music
cooking) a spicy tomato sauce.
an edible European plant (*Tragopogon*)
family, with a long root like that of a
PLANT. ▶ the root of this plant used as

Arms Limitation Talks.

on salt) sodium chloride (NaCl), which
gives seawater its characteristic taste
reserving food. ▶ poetic/literary something
quancy. ▶ a saltcellar. ▶ table salt mix-
garlic salt. 2 Chemistry any chemical
reaction of an acid with a base, with
the acid replaced by a metal or other
anion an experienced sailor. ▶ adj. [sɒl-
d with, or tasting of salt: salt water]
ing on the coast or in salt marshes. ▶
ed) season or preserve with salt: con-
ter. ▶ figurative make (something) plain
riddle (a road or path) with salt in order
fraudulently make (a mine) appear to
ch ore into it. 3 [as adj.] (salted) [sɒl-
a resistance to disease by surviving
adj.]

the (or someone's) wound made
painful for someone, the salt of
people of great kindness, reliability
biblical allusion to Matt 5:13: [salt]
(or pinch) of salt regard something
part of something. worth one's
b or profession specified.

nothing away informal secretly ston-
ey.
ked or speckled with intermingled
red-pepper hair.

1 Biology abrupt evolutionary change.
2 Geology the movement of hard ma-
terial in a turbulent flow of air or water.
[sɒl-] adj.
[sɒl-] adj. chiefly Entomology (esp. of
sapping.
ame house having up to three stories
he back with a steeply pitched roof.

a salt-tolerant orache plant sometimes
aline soils or to provide grazing in arid

(*Tamarix gallica*) with reddish-brown
foliage.
a container for storing salt, typically
ations.

3 structure in sedimentary rocks, formed
as been forced upward.
1 person dealing in or employed in
n whose work involved the preservation

: pools in which seawater is left to evaporate

at land covered with a layer of salt.
▶ n. grass (esp. *Distichlis spicata*) growing
aline regions.
northern Mexico, capital of the state of

sko/ ▶ n. a dish consisting of rolled
oked with herbs, bacon, and other

crisp, savory cracker sprinkled with

raldy another term for St. Andrew's
m) incorporating a motif based on the
wise f., w/z/ adv.

f Utah, in the northern part of the state
3 in 1847 by Brigham Young.
nals go to lick salt from the ground.
imals to lick.

ustal grassland that is regularly flooded

that is subject to flooding by seawater

ake in southeastern California; crosses
olorado River.

er or depression in the ground in which
a deposit of salt.

saltpeter /sɒlˈpi:tər/ (Brit. saltpetre) ▶ n. another term for POTAS-
SIUM NITRATE.

saltpwater /sɒlˈtɔːtər/ ▶ n. [sɒlˈtɔːtər] ▶ adj. [sɒlˈtɔːtər] of or found in salt wa-
ter; living in the sea: saltwater fish.

saltpwater crocodile ▶ n. a large and dangerous crocodile (*Cro-
codylus porosus*) occurring in estuaries and coastal waters from
southwestern India to northern Australia.

salwort /sɒlˈwɔːrt/ ▶ n. a plant (genus *Salsola*) of the
goosefoot family that typically grows in salt marshes. It is rich in al-
kali, and its ashes were formerly used in soap-making.

salty /sɒlˈti/ ▶ adj. (saltier, saltiest) tasting of, containing, or pre-
served with salt. ▶ (of language or humor) down-to-earth; coarse.

▶ informal tough; aggressive. —saltiness n.

salubrious /səˈluːbrɪəs/ ▶ adj. health-giving; healthy: salubrious
weather. ▶ (of a place) pleasant; not run-down. —salubriously
adv. —salubriousness n.; —salubrity /ˈbrɪti/ n.

salut /səˈluːt/ ▶ n. [səˈluːt] ▶ exclam. used to express friendly feelings to-
ward one's companions before drinking.

salutary /səˈluːtəri/ ▶ adj. (esp. with reference to something un-
welcome or unpleasant) producing good effects; beneficial.

salutation /səˈluːtəʃən/ ▶ n. a gesture or utterance made as a
greeting or acknowledgment of another's arrival or departure. ▶ a
standard formula of words used in a letter to address the person be-
ing written to. —salutationally /-tʃənəl/ adj.

salutatorian /səˈluːtəriən/ ▶ n. the student who ranks sec-
ond highest in a graduating class and delivers the salutatory.

salutatory /səˈluːtəri/ ▶ n. [səˈluːtəri] ▶ adj. (esp. of an address) relating to or
of the nature of a salutation. ▶ n. (pl. -ies) an address of welcome,
esp. one given as an oration by the student ranking second highest
in a graduating class at a high school or college.

salute /səˈluːt/ ▶ n. a gesture of respect, homage, or polite recogni-
tion or acknowledgment, esp. one made to or by a person when ar-
riving or departing. ▶ a prescribed movement, typically a raising of
a hand to the head, made by a member of a military or similar force
as a formal sign of respect or recognition. ▶ (often with adj.) the dis-
charge of a gun or guns as a formal or ceremonial sign of respect or
celebration. ▶ v. [trans.] make a formal salute to. ▶ greet. ▶ show or
express admiration and respect for. —saluter n.

Salvador /səˈveɪdər/ ▶ n. [səˈveɪdər] ▶ n. a city on the Atlantic coast of
eastern Brazil, capital of the state of Bahia; pop. 2,075,000. Former
name BAHIA.

Salvadoran /səˈveɪdərən/ ▶ n. [səˈveɪdərən] ▶ n. of or relating to El Salvador.

salvage /səˈveɪdʒ/ ▶ v. [trans.] rescue (a wrecked or disabled ship or its
cargo) from loss at sea. ▶ retrieve or preserve (something) from po-
tential loss or adverse circumstances. ▶ n. the rescue of a wrecked or
disabled ship or its cargo from loss at sea. ▶ the cargo saved from a
wrecked or sunken ship. ▶ the rescue of property or material from
potential loss or destruction. —salvageable adj.; —salvager n.

salvation /səˈlveɪʃən/ ▶ n. Theology deliverance from sin and its
consequences. ▶ preservation or deliverance from harm, ruin, or
loss. ▶ (one's salvation) a source or means of being saved in this
way: his only salvation was to outfly the enemy.

Salvation Army (abbr. SA) ▶ n. a worldwide Christian evangelical
organization on quasi-military lines. Established by William Booth,
it is noted for its work with the poor and for its brass bands. —sal-
vationism /-ˈnɪzəm/ n.; —salvationist /səˈlveɪʃənɪst/ n.

salve /sælv/ ▶ n. an ointment used to promote healing of the skin
or as protection. ▶ figurative something that is soothing or consoling
for wounded feelings or an uneasy conscience: the idea provided
him with a salve for his guilt. ▶ v. [trans.] archaic apply salve to. ▶ fig-
urative soothe (wounded pride or one's conscience): charity salves
our conscience.

salve2 /sælv/ ▶ v. archaic term for SALVAGE. —salvable /səˈlveɪbəl/
adj.

salver /səˈlveɪ/ ▶ n. a tray, typically one made of silver and used in
formal circumstances.

Salve Regina /səˈlveɪ ˈrɛɡɪnə/ ▶ n. a Roman Catholic hymn or
prayer said or sung after compline, and after the Divine Office from
Trinity Sunday to Advent.

salvia /səˈlveɪə/ ▶ n. a widely distributed plant (genus *Salvia*) of the
mint family, esp. (in gardening) a bedding plant cultivated for its
spikes of bright flowers.

salvo /səˈlveɪ/ ▶ n. (pl. -os or -oes) a simultaneous discharge of ar-
tillery or other guns in a battle. ▶ a number of weapons released
from one or more aircraft in quick succession. ▶ figurative a sudden,
vigorous, or aggressive act or series of acts: the pardons provoked a
salvo of accusations.

salvo-labile /səˈlveɪ ˈlæbl/ ▶ n. a scented solution of ammonium
carbonate in alcohol, used as smelling salts.

salvor /səˈlveɪər/ ▶ n. a person engaged in salvage of a ship or items
lost at sea.

Salween /səˈlveɪn/ ▶ n. a river in Southeast Asia that rises in Tibet and
flows for 1,500 miles (2,400 km) southeast and south through My-
anmar (Burma) to the Gulf of Martaban, an inlet of the
Andaman Sea.

Salvut /səˈlveɪt/ ▶ n. a series of seven Soviet manned orbiting space
stations, launched between 1971 and 1982.

Salzburg /ˈsɒlz.bɜːrg/ ▶ n. [ˈsɒlz-; ˈzɒltz.bɜːrk] a city in western Austria,
near the border with Germany, the capital of a state of the same
name; pop. 144,000. It is noted for its annual music festivals.

Salzgitte /ˈzɒltz.ɡɪtə/ ▶ n. an industrial city in Germany, in Lower
Saxony, southeast of Hanover; pop. 115,000.

SAM /sæm/ ▶ abbr. surface-to-air missile.

Sam. ▶ abbr. Bible Samuel.

samādhi /səˈmædhi/ ▶ n. (pl. samādhis) Hinduism & Buddhism a state
of intense concentration achieved through meditation. In Hindu
yoga this is regarded as the final stage, at which union with the di-
vine is reached (before or at death). ▶ Indian a funerary monument.

Samar /səˈmɑːr/ ▶ n. an island in the Philippines, southeast of Luzon. It
is the third largest island in the group.

Samarra /səˈmɪrə/ ▶ n. a city and river port in southwestern central
Russia, situated on the Volga River at its confluence with the Sam-
ara River; pop. 1,258,000. Former name (1935–91) KUIBYSHEV.

samarra /səˈmɪrə/ ▶ n. Botany a winged nut or achene con-
taining one seed, as in ash and maple.

Samarra /səˈmɪrə/ ▶ 1 an ancient city in central Palestine, found-
ed in the 9th century BC as the capital of the northern Hebrew king-
dom of Israel. The ancient site is situated in the modern West Bank,
northwest of Nablus. 2 the region of ancient Palestine around this
city, between Galilee in the north and Judaea in the south.

Samarinda /səˈmɑːrɪndə/ ▶ n. a city in Indonesia, in eastern Borneo;
pop. 265,000.

Samaritan /səˈmərɪtən/ ▶ n. (usu. good Samaritan) a
charitable or helpful person (with reference to Luke 10:33). 2 a
member of a people inhabiting Samaria in biblical times, or of the
modern community in the region of Nablus claiming descent from
them, adhering to a form of Judaism accepting only its own ancient
version of the Pentateuch as Scripture. 3 the dialect of Aramaic
formerly spoken in Samaria. ▶ adj. of or relating to Samaria or the
Samaritans. —Samaritanism /-ɪzəm/ n.

samarium /səˈmərɪəm/ ▶ n. the chemical element of atomic num-
ber 62, a hard, silvery-white metal of the lanthanide series. (Sym-
bol: Sm)

Samarqand /səˈmɑːr.kænd/ ▶ n. [səˈmɑːrˈkænd/ (also Samarqand) a
city in eastern Uzbekistan; pop. 370,000. One of the oldest cities in
Asia, it was founded in the 3rd or 4th millennium BC. It was a pros-
perous center on the Silk Road and, in the 14th century, became the
capital of Tamerlane's Mongol empire.

Sama Veda /səˈmɑː ˈvedə/ ▶ n. [ˈvedə/ Hinduism one of the four Vedas, a
collection of liturgical chants chanted aloud at the sacrifice. Its ma-
terial is drawn largely from the Rig Veda. See VEDA.

samba /ˈsæmbə/ ▶ n. [səˈm-] a Brazilian dance of African origin. ▶ a
piece of music for this dance. ▶ a lively modern ballroom dance imi-
tating this dance. ▶ v. (sambas, sambaed or sambad, sam-
baing /-bɔːɪŋ/) [intrans.] dance the samba.

sambal /ˈsæmbəl/ ▶ n. (in oriental cooking) hot relish made with
vegetables or fruit and spices.

sambar /ˈsæmbər/ ▶ n. a dark brown woodland deer (*Cervus
unicolor*) with branched antlers, of South Asia and the Philippines.

sambhar /ˈsæmbər/ ▶ n. a spicy southern Indian dish con-
sisting of lentils and vegetables.

Sambo /ˈsæmbə/ ▶ n. (pl. -os or -oes) 1 offensive a black person.
[ORIGIN: early 18th cent.; perhaps from Fula *sambo* 'uncle'.] 2 (sambo) historical a person of mixed race, esp. of black and Indian
or black and European blood. [ORIGIN: mid 18th cent.; from
American Spanish *zambo*, denoting a kind of yellow monkey.]

Sam Browne belt /sæm ˈbraʊn/ ▶ n. a leather belt with a support-
ing strap that passes over the right shoulder, worn by army and po-
lice officers.

sambuca /sæmˈbʊkə/ ▶ n. an Italian aniseed-flavored liqueur.

Same /səmeɪ/ ▶ plural n. variant spelling of SAMI.

same /səmeɪ/ ▶ adj. (the same) 1 identical; not different; unchanged:
he's worked at the same place for quite a few years | I'm the same
age as you are | [with clause] he put on the same costume that he had
worn in Ottawa. ▶ (this/that same) referring to a person or thing
just mentioned: that same year I went to Boston. 2 of an identical
type: they all wore the same clothes. ▶ pron. 1 (the same) the same
thing as something previously mentioned: I'll resign and encourage
everyone else to do the same. ▶ people or things that are identical or
share the same characteristics: there are several brands and they're
not all the same. 2 (chiefly in formal or legal use) the person or
thing just mentioned: sighted sub, sank same. ▶ adv. similarly; in the
same way: treating women the same as men | he gave me five dol-
lars, same as usual. —sameness n.

PHRASES all (or just) the same in spite of this; nevertheless: she
knew they had meant it kindly, but it had hurt all the same. ▶ In any
case; anyway: I can manage alone, thanks all the same. ▶ at the
same time 1 simultaneously. 2 on the other hand; nevertheless;
yet: it's a very creative place, but at the same time it's very relaxing.
be all the same to be unimportant to (someone) what happens; it
was all the same to me where it was being sold, by the same token
see TOKEN. one and the same the same person or thing (used for
emphasis): the guy in the glasses and Superman were one and the
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same.

sergeant-at-arms

declaring someone bankrupt. ■ a government spending. ■ Chancery. 2 the action of isolating.

any disk sewn as one of many official Venetian gold coins.

wood tree, esp. the California redwood.

national park in the Sierra Nevada established in 1890 to protect

-1843), Cherokee Indian scholar; Cherokee name *Sagoyew*; also. He invented a writing system. The giant sequoia trees of California.

ion.

dge of ice on the surface of a glacier.

l the women's apartments (harem) for HAREM (sense 2). 2 (the) ce, esp. the Sultan's court and government.

CARAVANSARY (sense 1).

■ a shawl or blanket worn at a

/-fim/ or seraphs) an angelic being in angelology as belonging to the celestial hierarchy, associated with

eristic of or resembling a seraph or graphically /-ik(a)le/ adv.

logy a god whose cult was developed a combination of Aps and Osiris; a common worship.

l of Serbia. ■ a person of Serbian origin, the Serbs, or their language.

Balkans, part of Yugoslavia; pop. 10-Croat; capital, Belgrade.

th Slavic language of the Serbs, written in the Cyrillic alphabet. See SERB. /-adj. of or relating to

in and ... Serbo-Croat. ■ relat-

krō/ (also Serbo-Croatian /krō/ language spoken in Serbia, Croatia, and Bosnia-Herzegovina. Serbo-Croat is generally comprised of two closely similar forms: Cyrillic, and Latin, written in the Latin script.

cession of plant (or animal) colonization habitat to the appropriate succession.

e of music sung or played in the night under the window of his lover.

l (trans.) entertain (someone) with

a cantata with a pastoral subject. ■ a cantata or wind band.

the occurrence and development of a disease. ■ a fortunate stroke of luck. /-dipit/ adj.; serendipitous

ful, and untroubled; tranquil; serene (title) used as a term of respect for a family: His Serene Highness. ■ a calm sea.

n Tanzania, west of the Great Rift here.

the state of being calm, peaceful, or happy. ■ (His/Your, etc., Serenity) a similar diglary.

bound under the feudal system to a lord. /-fij/ n.; serfdom /-dorm/ n. a coarse or worsted fabric. ■ v. [trans.] to prevent fraying.

uncommissioned officer in the army or Marine Corps) an NCO staff sergeant, or (in the US Air Force) a sergeant.

man and below staff sergeant. ■ a police officer. ■ a police officer. ■ a police officer.

gear/oy /-jans/ n. (pl. -ies). ■ at-arms)

sergeant Baker

1249

serpentine

Sergeant Baker /n. Austral. a brightly colored edible marine fish (*Aulopus purpurissatus*, family Aulopidae) with two elongated dorsal fin rays, occurring in warm Australian coastal waters.

Sergeant first class /n. a noncommissioned officer in the US Army of a rank above staff sergeant and below master sergeant.

Sergeant fish /n. another term for COBIA.

Sergeant major /n. 1 an noncommissioned officer in the US Army or Marine Corps of the highest rank, above master sergeant and below warrant officer. 2 a warrant officer in the British army.

3 a fish (*Abudefduf saxatilis*, family Pomacentridae) with boldly striped sides that lives in warm seas, typically on coral reefs.

Serger /'sɜːrʒə/ n. a sewing machine used for overcasting to prevent material from fraying at the edge.

Sergius, St. /'sɜːrʒəs/ (1314-92), Russian reformer and mystic; Russian name *Svyatol Sergi Radonezhsky*. He inspired the resistance that saved Russia from the Tatars in 1380.

Seriat /'sɜːriət/ n. 1 consisting of, forming part of, or taking place in a series: a serial publication. 2 Music using transformations of a fixed series of notes. 3 Computing (of a device) involving the transfer of data as a single sequence of bits. See also SERIAL PORT. 4 Computing (of a processor) running only a single task, as opposed to multitasking. 5 (of a criminal) repeatedly committing the same offense and typically following a characteristic, predictable behavior pattern: a suspected serial rapist. 6 (of a person) repeatedly following the same behavior pattern: he was a serial adulterer. 7 denoting an action or behavior pattern that is committed or followed repeatedly: serial killings | serial monogamy. 8 a story or play appearing in regular installments on television or radio or in a magazine or newspaper. 9 (usu. serials) (in a library) a periodical. —seriat /'sɜːriət/ n.; seriatly /'sɜːriətli/ adv.

Seriatism /'sɜːriətɪzəm/ n. Music a compositional technique in which a fixed series of notes, esp. the twelve notes of the chromatic scale, are used to generate the harmonic and melodic basis of a piece and are subject to change only in specific ways. The first fully serial movements appeared in 1923 in works by Arnold Schoenberg. See also TWELVE-TONE. —seriatist /'sɜːriətɪst/ n.; seriatism /'sɜːriətɪzəm/ n.

Seriatize /'sɜːriətaɪz/ v. [trans.] 1 publish or broadcast (a story or play) in regular installments. 2 arrange (something) in a series: each document sent to investors should be individually numbered or seriatized. 3 Music compose according to the techniques of serialism. —seriatization /'sɜːriətaɪzən/ n.

Seriat number /n. a number showing the position of an item in a series, esp. one printed on paper currency or on a manufactured article for the purposes of identification.

Seriat port /n. Computing a connector by which a device that sends data one bit at a time may be connected to a computer.

Seriate /'sɜːriət/ n. [trans.] arranged or occurring in one or more series. ■ v. [trans.] arrange (items) in a sequence according to prescribed criteria. —seriation /'sɜːriətən/ n.

Seriatim /'sɜːriətɪm/ n. [trans.] formal taking one subject after another in regular order; point by point: it is proposed to deal with these matters seriatim.

Sericulture /'sɜːrɪkjʊltʃər/ n. the production of silk and the rearing of silkworms for this purpose. —sericulturist /'sɜːrɪkjʊltʃərɪst/ n.

Seriemma /'sɜːriəmə/ n. a large, ground-dwelling South American bird (family Cariamidae) related to the bustards, with a long neck and legs and a crest above the bill.

Serious /'sɜːriəs/ n. (pl. same) a number of things, events, or people of a similar kind or related nature coming one after another: a series of lectures. ■ [usu. with adj.] a set of related television or radio programs, esp. of a specified kind: a new drama series. ■ a set of books, maps, periodicals, or other documents published in a common format or under a common title. ■ a set of games played between two teams. See also WORLD SERIES. ■ a line of products, esp. vehicles or machines, sharing features of design or assembly and marketed with a separate number from other lines: [as adj.] a series III SWB Land Rover. ■ a set of stamps, banknotes, or coins issued at a particular time or having a common design or theme. ■ [as adj.] denoting electrical circuits or components arranged so that the current passes through each successively. The opposite of PARALLEL. ■ Geology (in chronostratigraphy) a range of strata corresponding to an epoch in time, being a subdivision of a system and itself subdivided into stages. ■ Chemistry a set of elements with common properties or of compounds related in composition or structure. ■ Mathematics a set of quantities constituting a progression or having the several values determined by a common relation. ■ Phonetics a group of speech sounds having at least one phonetic feature in common but distinguished in other respects. ■ Music another term for TONE ROW.

Serious in series (of a set of batteries or electrical components) arranged so that the current passes through each successively.

Serif /'sɜːrɪf/ n. a slight projection finishing off a stroke of a letter, as in T contrasted with T. See illustration at FONT. —serified /'sɜːrɪfɪd/ adj.

Serigraph /'sɜːrɪgrəf/ n. a printed design produced by means of a silk screen. —serigrapher /'sɜːrɪgrəfər/ n.; serigraphy /'sɜːrɪgrəfi/ n.

Serlin /'sɜːrɪn/ n. a small Eurasian and North African finch (genus

Serinus) related to the canary, with a short bill and typically streaky plumage.

Serine /'sɜːrɪn/ n. Biochemistry a hydrophilic amino acid, $\text{CH}_3\text{OHCHNH}_2\text{COOH}$, that is a constituent of most proteins.

Serious /'sɜːriəs/ n. combining the serious and the comic; serious in intention but jocular in manner or vice versa. —serious /'sɜːriəs/ n.; seriously /'sɜːriəsli/ adv.

Serious /'sɜːriəs/ n. 1 (of a person) solemn or thoughtful in character or manner. 2 (of a subject, state, or activity) demanding careful consideration or application: marriage is a serious matter. 3 (of thought or discussion) careful or profound: serious consideration. 4 (of music, literature, or other art forms) requiring deep reflection and inviting a considered response. 5 acting or speaking sincerely and in earnest, rather than in a joking or halfhearted manner. 6 significant or worrying because of possible danger or risk; not slight or negligible: serious injury. 7 [informal] substantial in terms of size, number, or quality: he suddenly had serious money to spend. —seriousness /'sɜːriəsness/ n.; seriously /'sɜːriəsli/ adv.

Serjeant-at-arms /'sɜːrʒənt/ n. British spelling of SERGEANT-AT-ARMS.

Serjeant-at-law /'sɜːrʒənt/ n. (pl. serjeants-at-law) Brit., historical a barrister of the highest rank.

Serjeanty /'sɜːrʒənti/ n. (pl. -ies) Brit., historical a form of feudal tenure conditional on rendering some specified personal service to the monarch.

Sermon /'sɜːrmən/ n. a talk on a religious or moral subject, esp. one given during a church service and based on a passage from the Bible. ■ a printed transcript of such a talk. ■ informal a long or tedious piece of admonition or reproof; a lecture. —sermon /'sɜːrmən/ n.; sermonize /'sɜːrmənaɪz/ v.

Sermonette /'sɜːrmənet/ n. a short sermon.

Sermonize /'sɜːrmənaɪz/ v. [intrans.] compose or deliver a sermon. ■ deliver an opinionated and dogmatic talk to someone. —sermonizer /'sɜːrmənɪzər/ n.

Sermon on the Mount /n. the discourse of Jesus recorded in Matt. 5-7, including the Beatitudes and the Lord's Prayer.

Serotype /'sɜːraɪp/ n. a form relating to serum: serotype. ■ involving a serous membrane: serositis.

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CERTIFICATE OF SERVICE

I, Andrew A. Lundgren, Esquire, hereby certify that on August 11, 2008, I caused to be electronically filed a true and correct copy of the foregoing document with the Clerk of the Court using CM/ECF, which will send notification that such filing is available for viewing and downloading to the following counsel of record:

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